

EECS 203 HW7 Solution

1.

(a) (5 pts)

“BANKSEL TRISA” is a directive.

“CLRF TRISA” and “COMF TRISA, F” are instructions.

(b) (5 pts)

The overall effect of this sequence is that it sets all the bits in the register TRISA to 1.

(c) (5 pts)

At some time during the execution of the instructions, the port may be driven by both the CPU and the external driver, which leads to a short.

(d) (5pts)

Notice the clock cycle is different from CPU cycle, the latter is made up of 4 clock cycles. So the dangerous condition could exist for 1 CPU cycle that is 4 clock cycles, 1.33 microseconds.

(e) (5 pts)

```
BANKSEL TRISA
MOVLW 0xFF
MOVWF TRISA
```

(f) (5 PTS)

```
BCF STATUS, RP1
BSF STATUS, RP0
MOVLW 0xFF
MOVWF TRISA
```

(g) (5 pts)

```
01 0011 0000 0011
01 0110 1000 0011
11 0000 1111 1111
00 0000 1000 0101
```

2.

(a) (5 pts.)

Since the short loop needs to be executed 3000 times, if it is written inside one loop, we need a counter to store the value 3000. This can't be done with 8-bit registers, which can store a maximum number of 255. Another solution is to write a lengthy code, but of course we don't want that.

(b) (10 pts)

```
LOW_TICK 0x20
HIGH_TICK 0x21
REAL_TICK 0x22
    DELAY_LOOP:
    MOVWF REAL_TICK
    REAL_WAIT_LOOP
        MOVLW d'10'
        MOVWF HIGH_TICK
        LONG_WAIT_LOOP
```

```
    MOVLW d'100'  
    MOVWF LOW_TICK  
    SHORT_WAIT_LOOP  
        NOP  
        NOP  
        NOP  
    DECFSZ LOW_TICK, F  
    GOTO SHORT_WAIT_LOOP  
DECFSZ HIGH_TICK, F  
GOTO LONG_WAIT_LOOP  
DECSFZ REAL_TICK, F  
GOTO REAL_WAIT_LOOP  
RETURN
```

3.

(5 PTS) The register INDF can be accessed for indirect addressing while the register FSR is the indirect address. For example, instead of specifying a particular register, if INDF is specified, the value stored in FSR will be used in whatever instruction specified INDF.