ECE 303: Advanced Digital Logic Design
Final Exam

5 June 2006

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1. **(15 pts.)** For each of these questions, please limit your answer to a short paragraph.

   (a) Why are most existing sequential digital logic designs synchronous?

   (b) Why is integrated circuit power dissipation important?

   (c) Can reducing frequency, alone, decrease the energy requirements to complete a task? Why or why not?

2. **(30 pts.)** Design a synchronous finite state machine that will output a 1 if and only if it has had three or more 1 inputs.

   (a) Write a regular expression for the specified behavior.

   (b) Show the state diagram for a machine meeting these requirements.

   (c) Show the state table for a machine meeting these requirements.

   (d) Minimize the machine, or prove that it is minimal.

   (e) Do state assignment.

   (f) Determine the state variable and output functions.

   (g) Prepare the functions for implementation with CMOS.

   (h) Show the gate-level schematic of the machine.

   (i) Show the transistor-level implementation of each type of gate in the machine. Use hierarchy.

   (j) Show the transistor-level implementation of each type of flip-flop in the machine. Use hierarchy.

3. **(20 pts.)** A *lag-flop* is a single-input flip-flop with the following behavior. When the clock signal is high, the lag-flop outputs the value of the input at the previous falling clock edge. When the clock signal is low, the lag-flop outputs a zero.

   (a) Show the state diagram for a lag-flop.

   (b) Show the state table for a lag-flop.

   (c) Minimize the machine, or prove that it is minimal.

   (d) Do state assignment.

   (e) Determine the state variable and output functions.

4. **(15 pts.)** Use kernel extraction to minimize the following function:

$$f(a,b,c,d) = \sum(0,6,7,9,10,11,13,14) \tag{1}$$

5. **(10 pts.)** Show the transistor-level diagram for a Schmitt trigger inverter implemented in CMOS. Indicate which gates should be narrow.

6. **(10 pts.)** Consider the following VHDL code.

```
ENTITY dsgn IS
  PORT(a, b, c, d: in bit;
    e: out bit
  );
END dsgn;

ARCHITECTURE arch1 OF dsgn IS
  SIGNAL f: bit;
BEGIN
  MISC: process (a, b, c, d)
  begin
    if (a = '1') then
      e <= '1';
      f <= '1';
    elsif (b = '1') then
      e <= '0';
      f <= '0';
    elsif (c'event and c = '0') then
      e <= '0';
      f <= d;
    elsif (c'event and c = '1') then
      e <= f;
    end if;
  end process MISC;
END arch1;
```

(a) Describe or name this device.

(b) Describe or name signals *a*, *b*, *c*, *d*, and *e*.