

Homework three

EECS 303: Advanced Digital Logic Design
Fall 2008

Assigned 28 Oct
Due 4 Nov

You may discuss the assignment with your classmates. However, you need to write down your solutions independently. Please make sure your answers are legible. You can manually produce the circuit diagrams or use a graphics package with a logic gate library, e.g., `xfig`.

1. **(15 pts)** Given the following expression

$$L(A, B, C, D, E) = ABC + BCD + ABD + CDE$$

- List all of the kernels that may be extracted from L .
- Factor by the kernel for which the result will contain the fewest number of literals. Break ties by considering the difficulty of simplifying the resulting remainders. Identify kernels for each SOP sub-expression and factor until this is no longer possible. List the initial and final number of literals in L .

2. **(10 pts)** Given the following function of three inputs

$$F(A, B, C) = A \bar{B} \bar{C} + \bar{A} \bar{C} + \bar{A} B$$

- Draw a circuit diagram for an implementation of the function using a minimal number of NAND gates. You may assume access to complemented input variables but may not assume implicit negation of the output. Indicate the number of PMOS and NMOS transistors.
- Draw a circuit diagram for an implementation of the function using a minimal number of NOR gates. You may assume access to complemented input variables but may not assume implicit negation of the output. Indicate the number of PMOS and NMOS transistors.
- Implement the function using CMOS transmission gates (TGs). How many NMOS and PMOS transistors are required?

3. **(10 pts)** Given the following function of four inputs

$$F(A, B, C, D) = \bar{A} B C + A D + A C$$

- Implement it using an 8:1 multiplexor.
- Implement it using a 4:16 decoder and an OR gate.
- Implement the logic using a ROM. You may either draw the schematic or give a table showing the ROM contents.

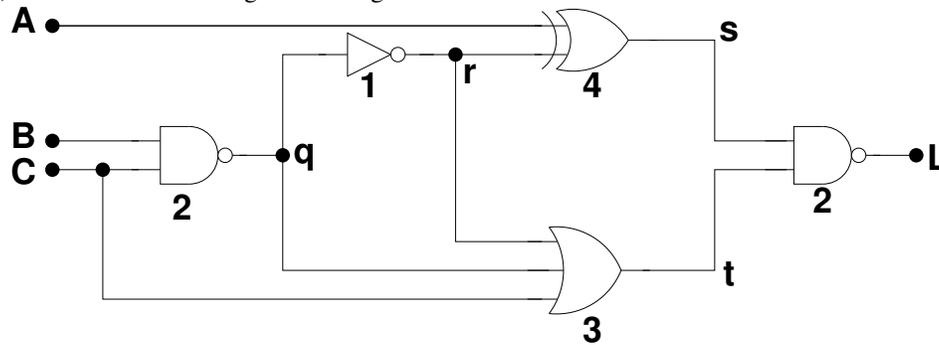
4. (15 pts) Given the following functions, use kernel extraction for multilevel minimization. In each case, count the number of literals in the original and final expression.

- (a) $G = AC + ADE + BC + BDE$
- (b) $G = ACD + BC + ABE + BD$
- (c) $G = AD + AE + BD + BE + CD + CE + AF$
- (d) Is kernel extraction optimal?

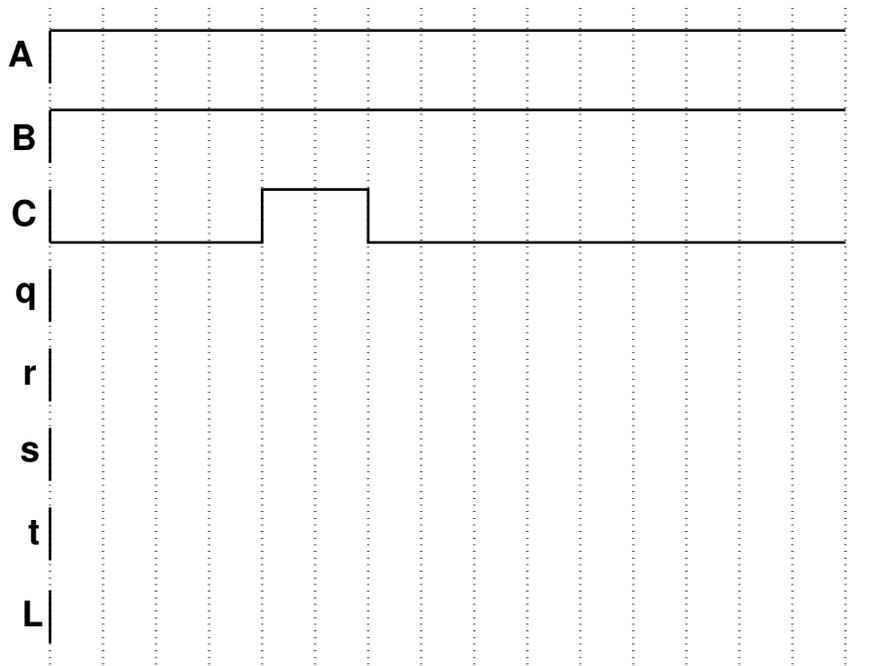
5. (5 pts) Contrast the following

- (a) Graph
- (b) Directed graph
- (c) Directed acyclic graph
- (d) Tree

6. (20 pts) Examine the following circuit diagram:



- (a) Each gate in the diagram is labeled with the number of time units it takes a signal change on any input to propagate to the output (and to the level of gates). Given that the inputs, A , B , and C are ready at time 0 and that the output, L , must be ready by time 7, calculate the slack at each gate. Does this circuit meet its timing constraints? If not, which gates would it be beneficial to speed up?
- (b) Assuming access to complemented and uncomplemented literals, reimplement the function using only those gate types shown in the figure. Minimize the circuit's delay. For example, you can use any number of XOR2 gates, each of which has a delay of four. However, you can't use any NOR3 gates because none exist in the diagram. Report your worst-case input to output delay.



(c) In the original circuit, use the above grid to draw the timing diagram for each signal, given the indicated input transitions. Indicate undefined values with shaded boxes.