

## Quiz 3:

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1. What are the *two* reasons to implement a logic function using multiple levels instead of just building one big gate?

2. Indicate the structure of a CMOS implementation of the following function, and assign a size for each transistor to achieve balanced delay given that the minimum-size transistor is of width  $k$ .

$$f(a, b, c) = \bar{a}\bar{b} + \bar{c}.$$

3. What are the qualitative concepts that guide gate sizing?