EECS 312: Digital Integrated Circuits
Lab Project 4 – Interconnect and sizing

Teacher:	Robert Dick
Assigned:	29 October
Due:	7 November

1 Elmore delay

Please use the Cadence tools to simulate the delay of the resistive–capacitive network in Figure 4–12 on page 153 of the textbook. You may assume that each capacitance is 100 fF and that each resistance is 10 Ω. Indicate the difference between the delay yielded using Elmore delay approximation and that for the simulation results. R_2 and R_4 have no impact on the Elmore delay time constant approximation. What happens to the simulation results when these two resistances are doubled? What happens to the simulation results when these two resistances are halved?

Deliverables

1. Timing diagrams for each of the three circuits considered.
2. Elmore and simulated delays for each of the three circuits considered.
3. An explanation of the differences between the Elmore delays and the simulated delays.

2 Sizing

Design a circuit implementing the following logic function:

$$f(a, b, c) = \overline{a} + \overline{b}\,\overline{c}$$

The raw inputs are $\overline{a}$, $\overline{b}$, and $\overline{c}$, which must pass through inverters with NMOSFET widths of 360 nm and PMOSFET widths of 720 nm. The raw inputs may change instantly. Delay is measured from the raw input 0.5 V_{DD} crossing to output 0.5 V_{DD} crossing.

Your first step will be designing the simplest balanced implementation of the function possible, without an inverter chain for driving the resistive–capacitive load. Calculate the delay of this design.

Next, size transistors or gates used in implementing the logic function, and design an inverter chain to minimize worst-case delay when driving a distributed resistive–capacitive load of 185 Ω–1.5 pF. It is acceptable to divide the load into segments in order to distribute drivers. However, no more than three load segments may be used. You may use as many levels of logic as desired in the function implementation.

You have the freedom to change the following portions of your design.

1. Function implementation style.

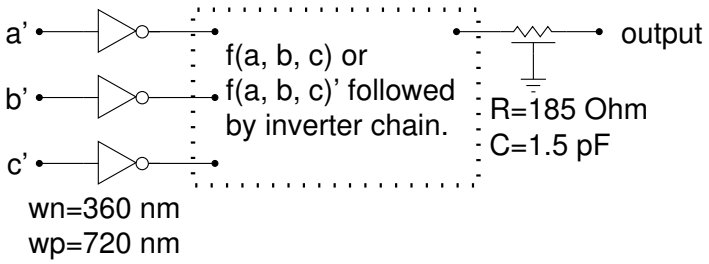

Figure 1: Circuit environment.

2. The number of inverters in the inverter chain.
3. Transistor sizings in function implementation and inverter chain.
4. Number of resistive–capacitive load segments in the range from one to three. An inverter may be inserted before each stage.

You may not change the following portions of the design.

1. The sizes of the first-stage inverters.
2. The implemented function, e.g., by producing an inverted version.
3. The number of resistive–capacitive load segments above three.
4. V_{DD}.
5. Resistive-capacitive load wire width.

Figure 1 depicts the environment in which your circuit will operate. I suggest the following design process. First, use your knowledge from lecture and reading to design a fast circuit. Then iteratively adjust transistor and/or gate sizes based on feedback from the simulation process.

Deliverables

1. Schematic of all circuit, including the raw inputs and resistive–capacitive loads.
2. Timing diagram for input transition(s) with worst-case propagation delays and rise/fall times for the simple and optimized designs. The timing diagram should show the raw inputs and the output. Please invert the printout so that the background is light and the lines are dark.
3. The energy-delay product for one transition causing a worst-case propagation delay, considering the time interval from input transition to the output coming within 10% of its steady-state value (i.e., 10% if the output is falling, 90% if the output is rising). Optimizing the energy-delay product will not influence your grade, but those who decide to optimize it despite this fact should note this in their reports. Those with high-quality designs will win accelerated lessons on fundamental-mode asynchronous finite state machine synthesis (this is graduate-level switching and sequential networks topic).
4. An explanation of why the transitions you considered are sure to contain the worst-case transition.
5. An explanation of each design decision and the work done during the design process.