EECS 312: Digital Integrated Circuits
http://ziyang.eecs.umich.edu/~dickrp/eecs312/

Robert Dick

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Instructor	Robert Dick http://robertdick.org/ dickrp@eecs.umich.edu 2417-G EECS Office hours: Tuesdays and Thursdays, 16:30–17:30
Lecture	1303 EECS Tuesdays and Thursdays, 15:00-16:30
Discussion	1690 EECS Fridays, 12:30–13:30
Teaching assistant	Amir Borna Email: aborna@umich.edu

1 References

Textbook

J. Rabaey, A. Chandrakasan, and B. Nikolic. *Digital Integrated Circuits: A Design Perspective*. Prentice-Hall, second edition, 2003.

Supplementary Texts

- Ben G. Streetman. *Solid State Electronic Devices*. Prentice-Hall, NJ, fifth edition, 2005.
- Andrei Vladimirescu. *The SPICE Book*. John Wiley & Sons, second edition, 1994.
- Adel S. Sedra and Kenneth C. Smith. *Spice for Microelectronic Circuits*. Harcourt School, third edition, 1991.
- Ivan Sutherland, Robert F. Sproull, and David Harris. *Logical Effort: Designing Fast CMOS Circuits*. Morgan Kaufmann, first edition, 1999.

2 Homework Assignments and Projects

Homework assignments are due at the beginning of lecture. There will be a 10% penalty per day for late assignments. No credit will be granted for assignments that were already covered in a discussion session (on Friday). Note that there the penalty for late assignments is gradual. If you neglect to leave some slack and

something unexpected comes up, you have the option of handing in the assignment a day late instead of staying up all night. There is no excuse for copying someone else's work.

There will be a number of software laboratory assignments and a final project. Laboratory assignments are subject to a 10% per day late penalty. There will be little if any slack in the final project due date so that deadline is hard.

Our grader will provide limited feedback on assignments. The GSI and I will selectively read more complex problems and laboratory projects to gauge progress and provide more detailed feedback. We will also provide solutions and be available for help with assignments and projects during office hours.

3 Purpose of Course and Course Objectives

Digital Integrated Circuits, is a junior-level digital circuits course for both electrical and computer engineering majors. Building upon pre-existing knowledge of MOSFET device operation, the student will learn to analyze and design digital circuits in various logic families, including static CMOS, domino, pass-transistor and sequential logic. Tradeoffs among these logic families will be emphasized (e.g., noise immunity vs. speed, density vs. static power), allowing students to make informed decisions on when to use each style. They will be introduced to SPICE simulators and will use SPICE heavily in designing various blocks of logic in lab assignments as well as a design project. Key memory structures (ROM, SRAM, and DRAM) will be described. This class will prepare students for EECS 427. The course has the following objectives.

1. Teach students the analysis and design of static CMOS digital circuits.
2. Develop a thorough understanding of the static and dynamic characteristics (delay, power, noise immunity, and density) of various MOS based logic families (CMOS, pseudo-NMOS, pass transistor, and domino).
3. Introduce and familiarize students with circuit simulation tools (SPICE) that will be invaluable to them in later courses (e.g., EECS 427) and industry as circuit designers.
4. Provide students the chance to work on small design projects where they attempt to minimize certain objective functions while meeting other design constraints for a functional unit. Collaborative discussion during the design process will be encouraged.
5. Teach the operation and importance of memory structures (ROM, SRAM, and DRAM) in large digital systems.
6. Provide students with the required knowledge to make informed decisions on when to use different logic styles and the tradeoffs inherent in those decisions.
7. Teach students to analyze the effect of interconnect parasitics on circuit performance.
8. Introduce students to important future trends in large-scale digital circuit design, including manufacturability issues and barriers to device scaling.

4 Topics

We will endeavor to cover the following topics. Time allocation will be adjusted based on rate of learning. References to relevant book chapters or supplements will be provided for each topic.

- Course overview and administrative details
- Context for digital integrated circuit design
- Scaling and process variation
- Transistor static behavior
- Transistor dynamic behavior
- Fabrication
- SPICE models
- CMOS inverters
- Inverter dynamic behavior
- Inverter power consumption
- CMOS gates
- Pass transistor logic
- Transmission gates
- Transistor and logic gate sizing
- Dynamic logic
- Domino logic
- np-CMOS
- Interconnect behavior
- Interconnect design
- Latches
- Flip-flops
- Other sequential elements
- ROM
- SRAM
- DRAM
- Future trends

5 Grade Weightings

- Homework: 20%
- Projects: 30%
- Midterm exams: 23%
- Final exam: 27%

6 The Line Between Collaboration and Copying

We will do our best to assign credit in proportion to contribution.

For group assignments, any student may discuss the problem and design ideas with any other students. However, the task of preparing, evaluating, and reporting on a group's design may only be divided among the members of the group. We will make the (unfortunately sometimes inaccurate) assumption that all group members have equal contribution.

For individual assignments, any student may discuss the problem and design ideas with any other students. However, students are individually responsible for preparing, evaluating, and reporting on their designs.

In summary, you are encouraged to share ideas and discuss assignments, but are not permitted to copy the schematics, simulation results, or reports of other students. If you feel that you must do this, report it openly so credit can be appropriately adjusted (removed). Continued participation in the course implies that you understand that discussion is fine but claiming credit for copied work is cheating.