Embedded Systems: An Application-Centered Approach

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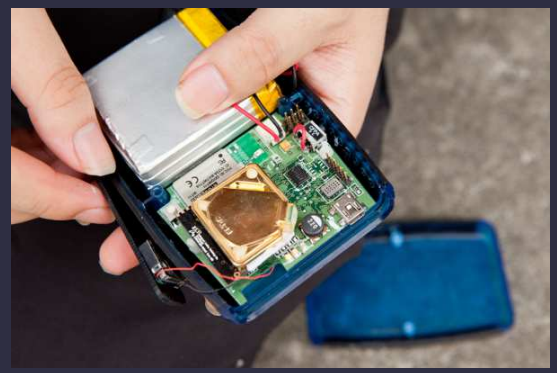


Two major sources of changing problems

New implementation technologies.

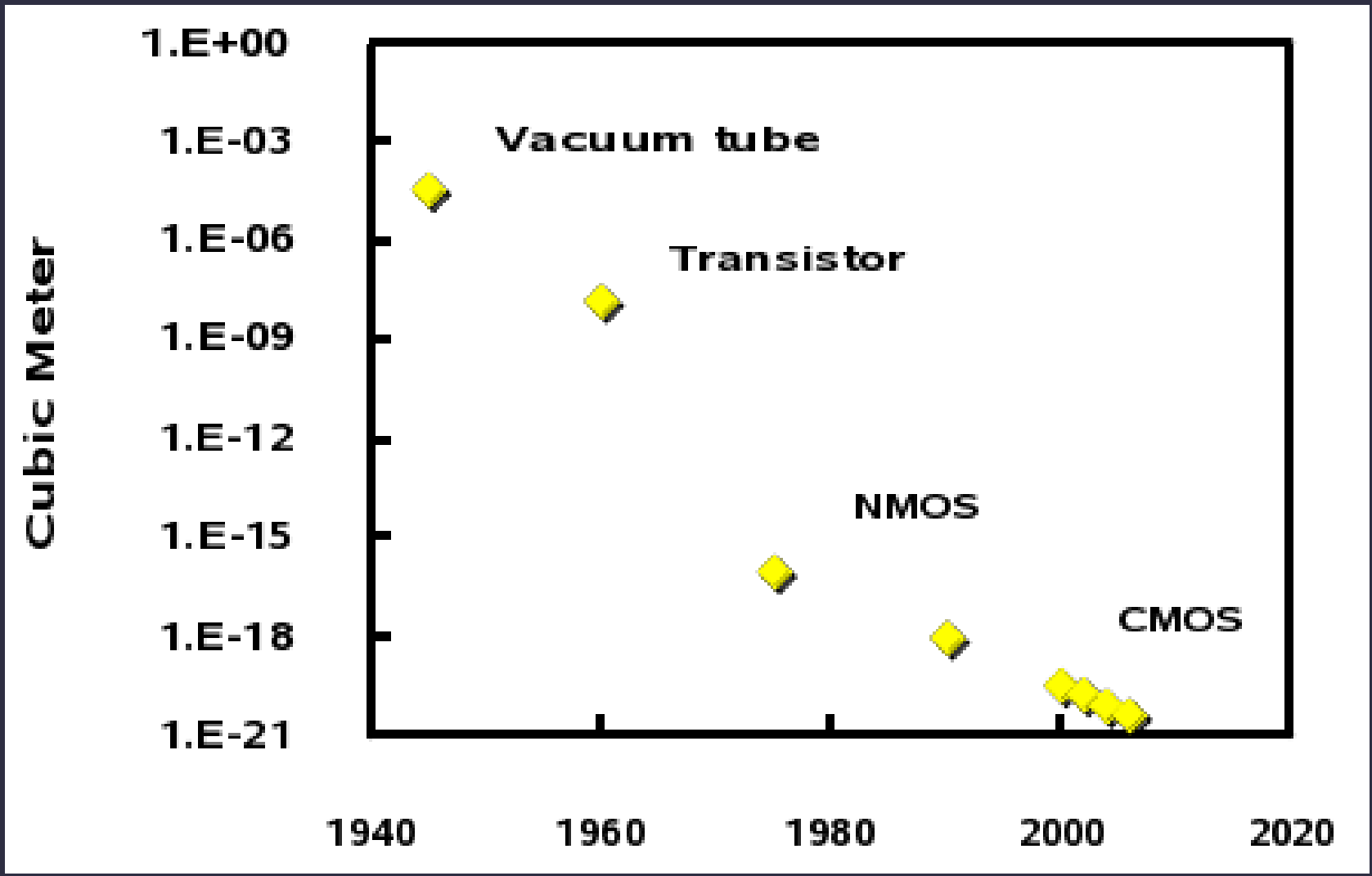
New applications.

Outline

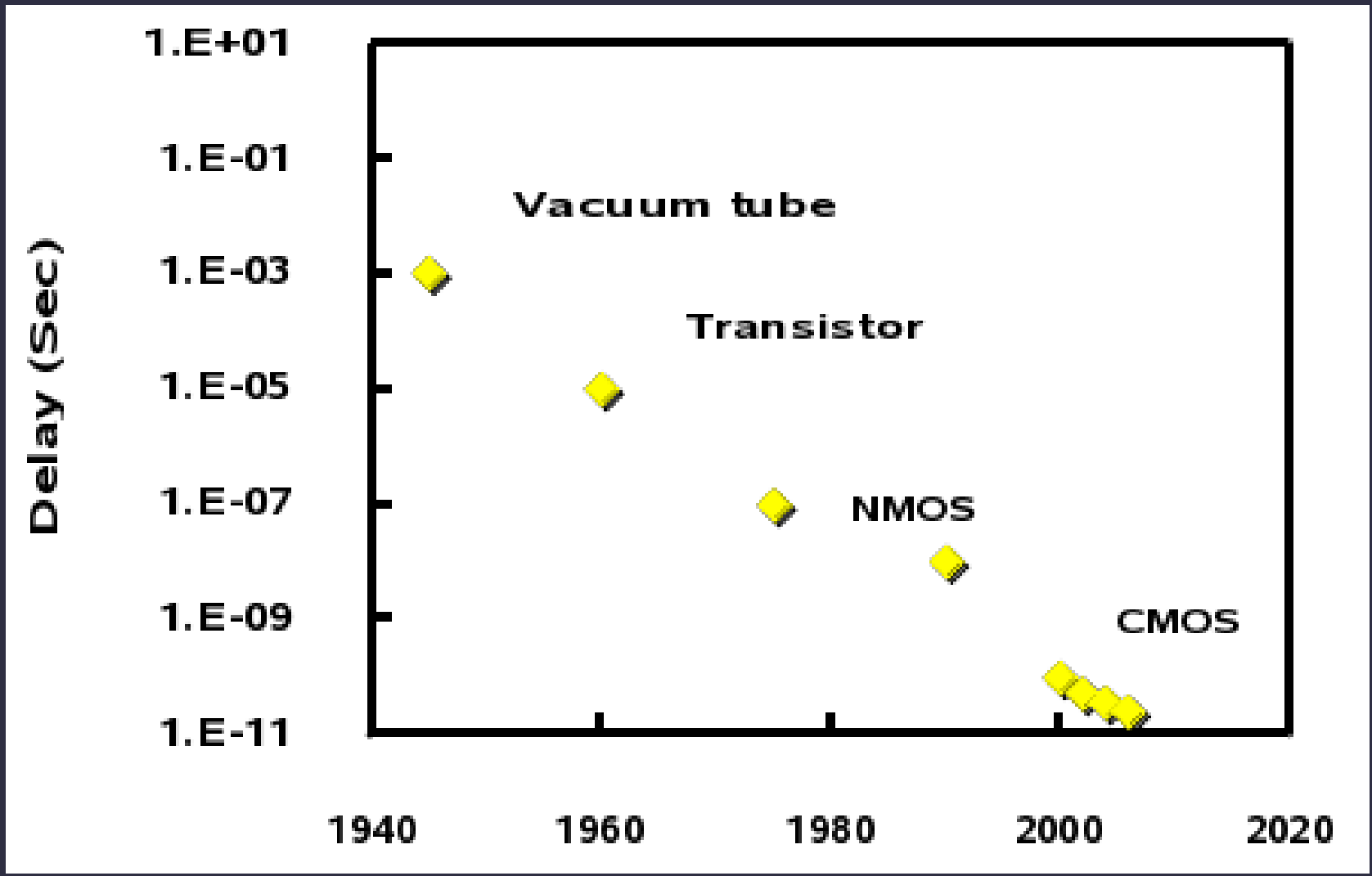
Evolution of computation

- 1800s: Mechanical
- Late 1800s–early 1900s: Electro-mechanical
- Early 1900s–mid 1900s: Vacuum tube electronic
- Mid 1900s–late 1900s: Bipolar (TTL)
- Late 1900s–early 2000s: MOS

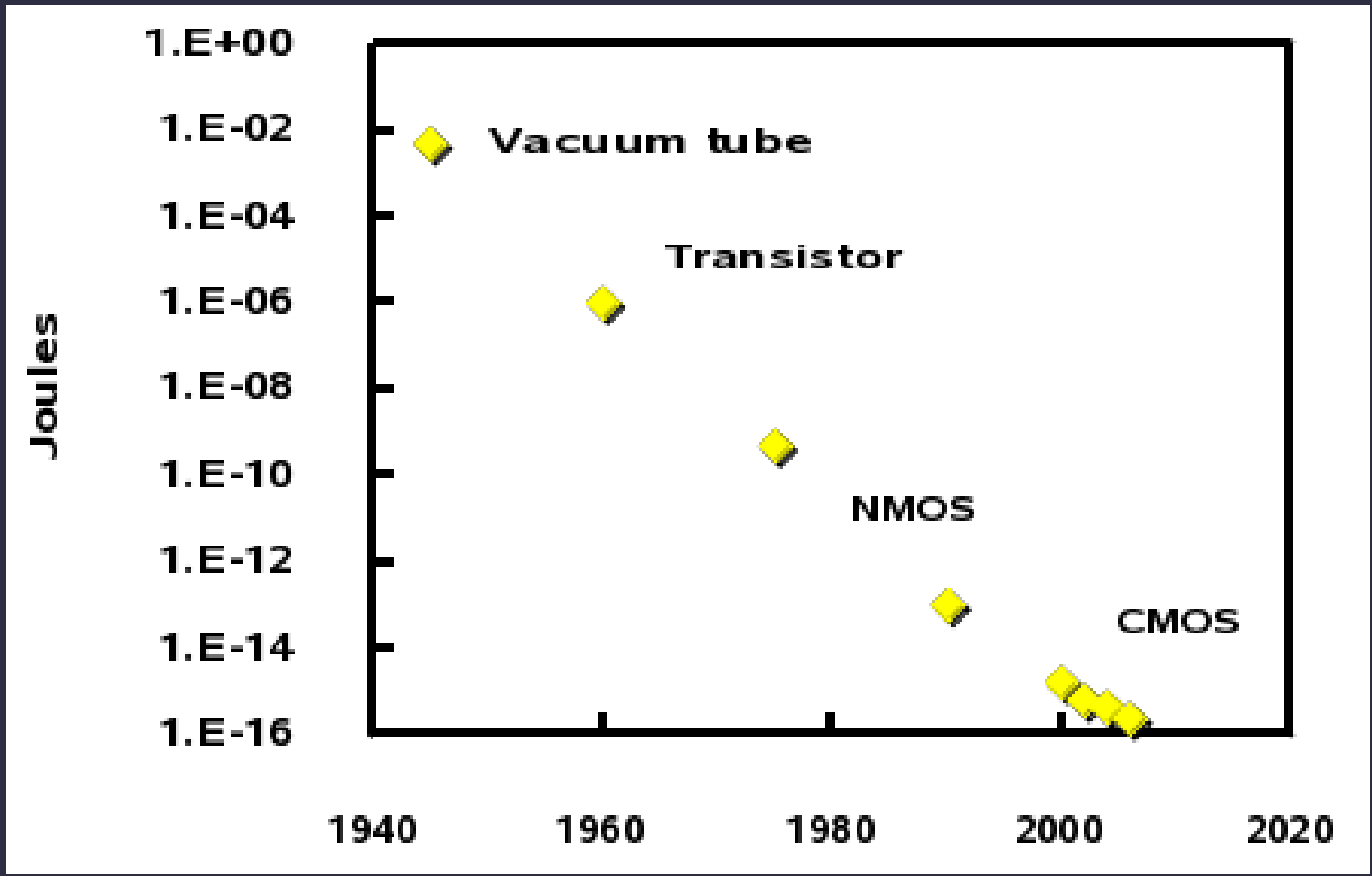
Impact of scaling on volume



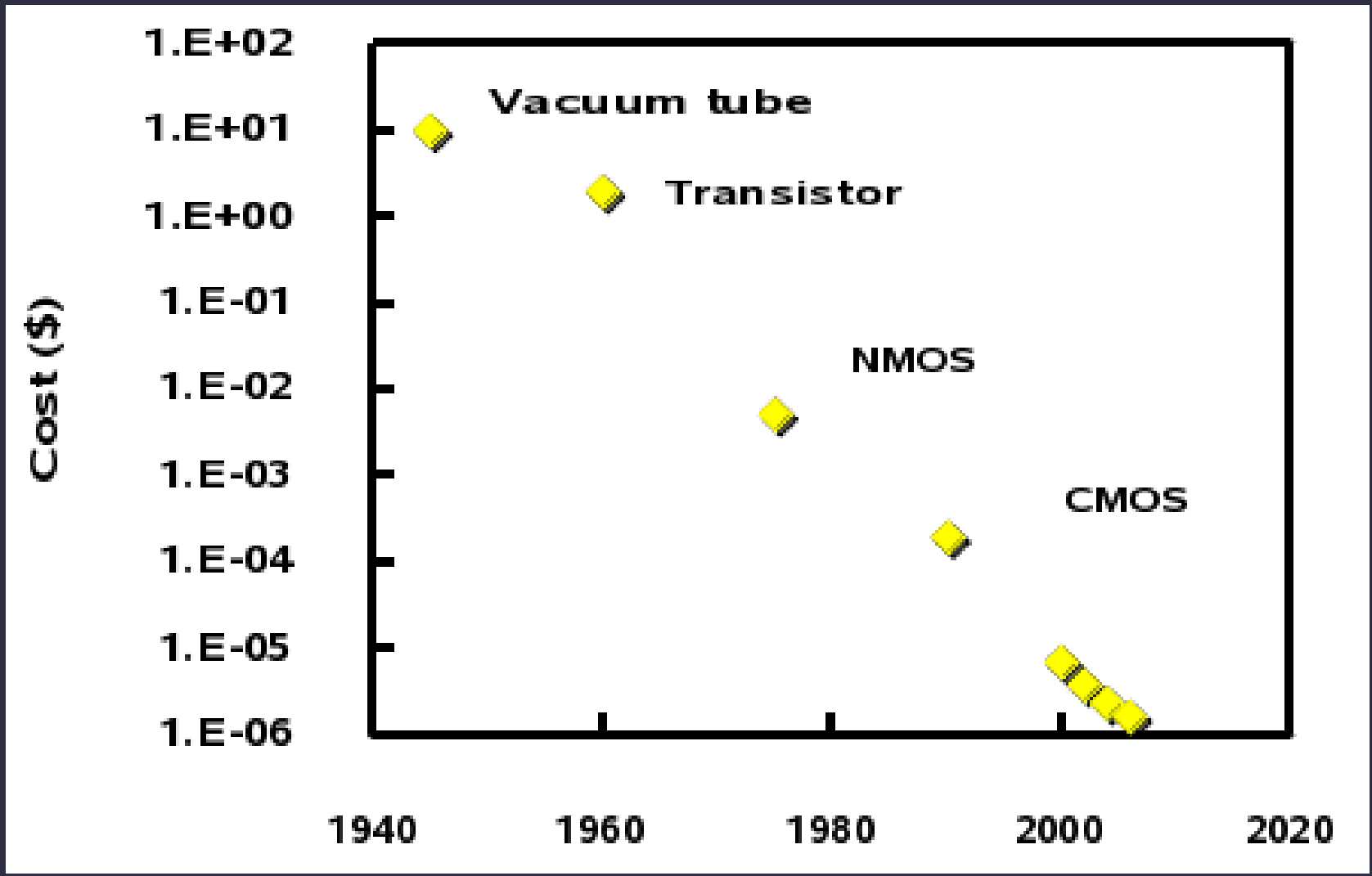
Impact of scaling on delay



Impact of scaling on energy consumption



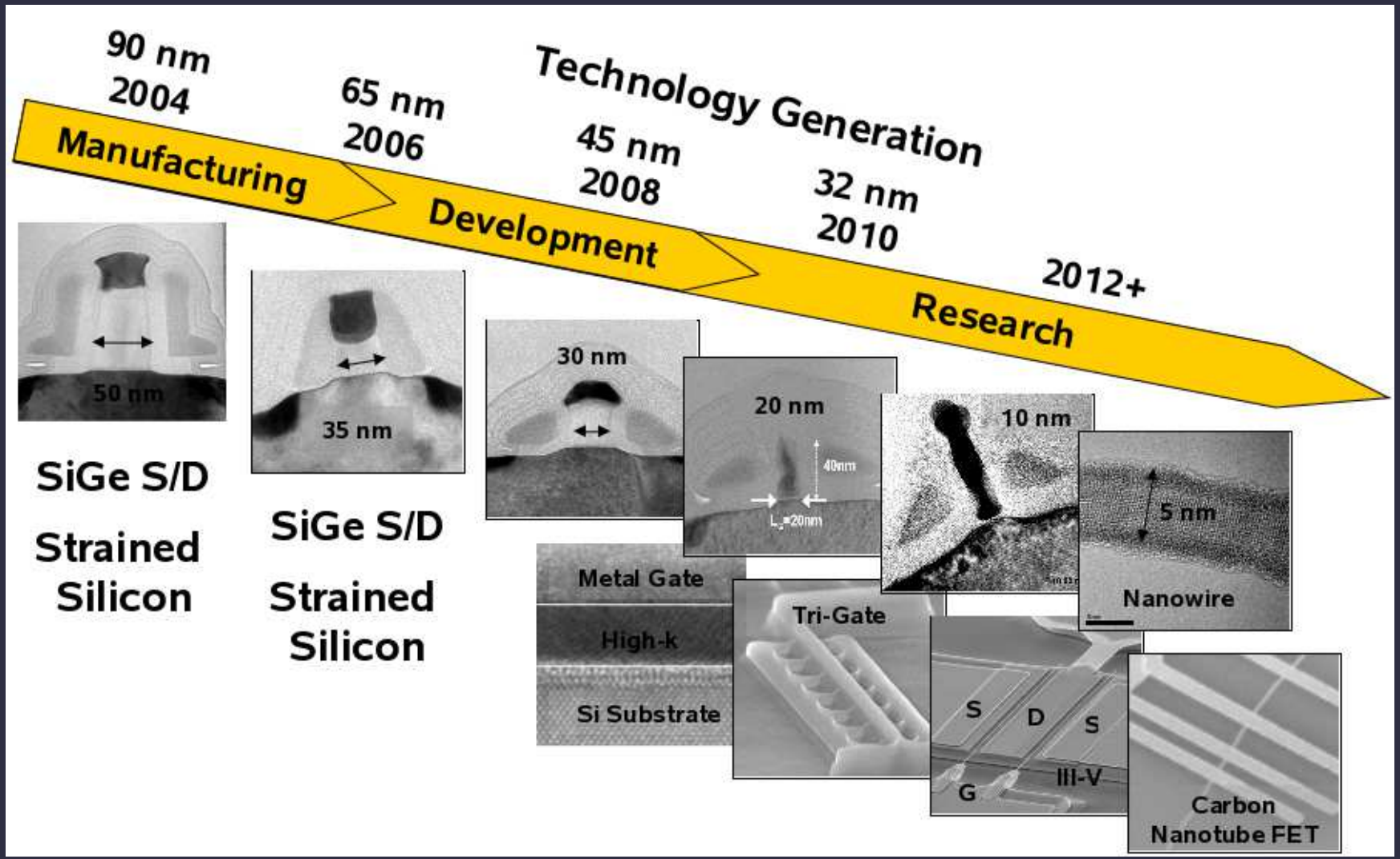
Impact of scaling on price



Scaling trends

High Volume Manufacturing	2004	2006	2008	2010	2012	2014	2016	2018
Technology Node (nm)	90	65	45	32	22	16	11	8
Integration Capacity (BT)	2	4	8	16	32	64	128	256
Delay = CV/I scaling	0.7	~0.7	>0.7	Delay scaling will slow down				
Energy/Logic Op scaling	>0.35	>0.5	>0.5	Energy scaling will slow down				
Bulk Planar CMOS	High Probability						Low Probability	
Alternate, 3D etc	Low Probability						High Probability	
Variability	Medium			High			Very High	
Inter-lr dielectric k	~3	<3	Reduce slowly towards 2-2.5					
RC Delay	1	1	1	1	1	1	1	1
Metal Layers	6-7	7-8	8-9	0.5 to 1 layer per generation				

Device trends



Advantages of CMOS relative to prior technologies

- Performance
- Gain, low noise
- Area
- Massive integration
- Power
- Reliability
- Fabrication difficulty & cost

Current status for CMOS

- 32 nm
- Power, thermal problems severe
- Fabrication cost per design high
- Potential reliability problems in future
- Soft errors
- Electromigration, dielectric breakdown, etc.
- Process variation
- Soon: Discrete dopant problems

Computing trends applications

- Increased market volume and size for portable and embedded systems compared to general-purpose computers.
- Instructor's opinion: Embedded will grow in importance in the future.
- High-performance general-purpose computing will still matter.
- Much of the general-purpose computation will move to data centers.

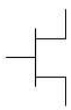
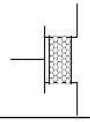
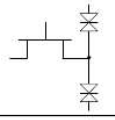
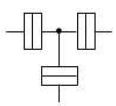
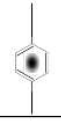
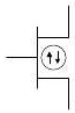
Advantages of alternative nanotechnologies

May allow continued process scaling after CMOS scaling impractical.

- Candidates
- Carbon nanotube
- Nanowire Single electron tunneling transistors

Comparison of nanoscale technologies

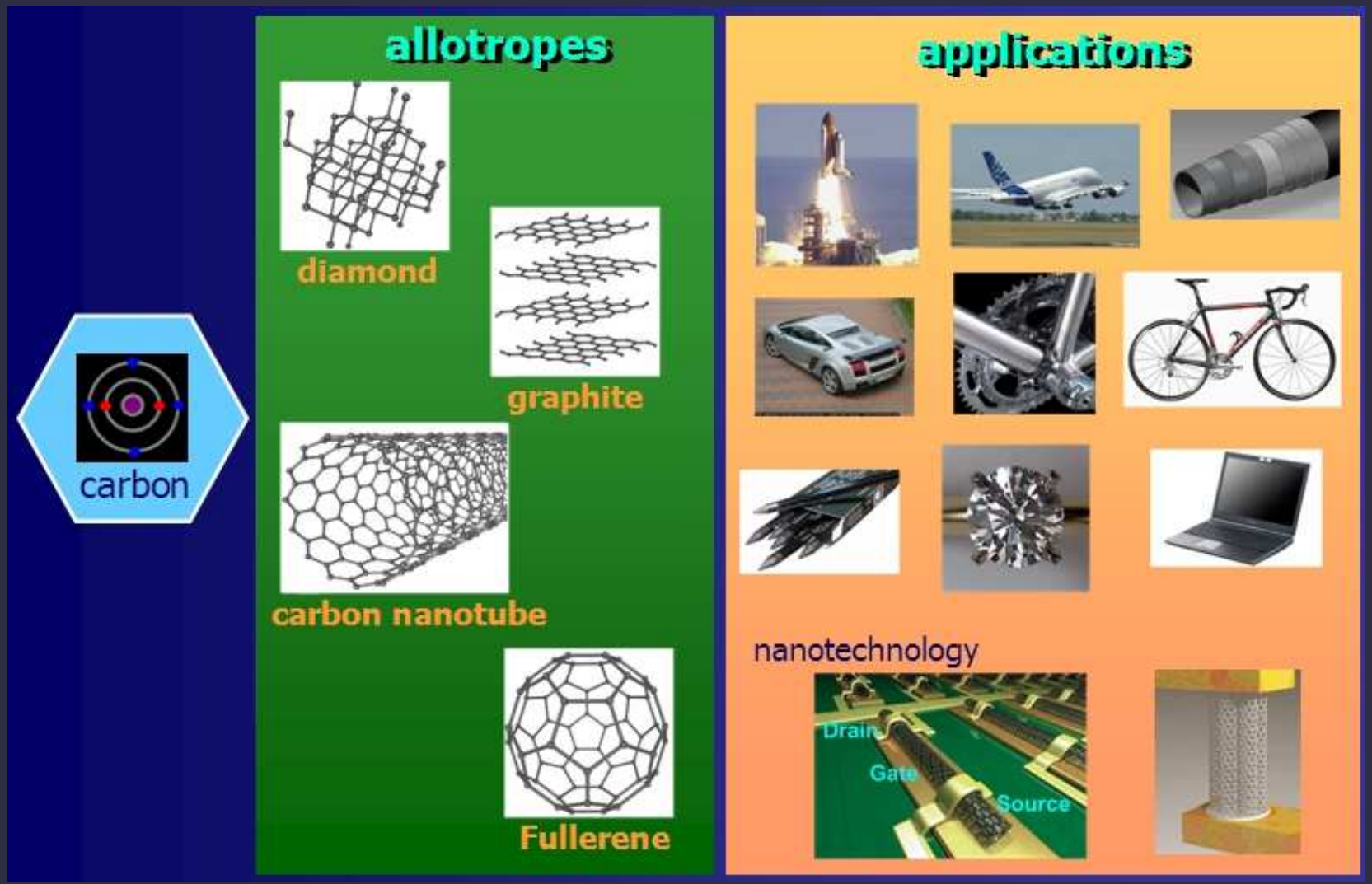
Table 59 Emerging Research Logic Devices—Demonstrated Projected Parameters

Device		 FET [B]	 1D structures	 Resonant Tunneling Devices	 SET	 Molecular	 Ferromagnetic logic	 Spin transistor
Types		Si CMOS	CNT FET NW FET NW hetero-structures Crossbar nanostructure	RTD-FET RTT	SET	Crossbar latch Molecular transistor Molecular QCA	Moving domain wall M: QCA	Spin transistor
Supported Architectures		Conventional	Conventional and Cross-bar	Conventional and CNN	CNN	Cross-bar and QCA	CNN Reconfigure logic and QCA	Conventional
Cell Size (spatial pitch)	Projected	100 nm	100 nm [C]	100 nm [C]	40 nm [L]	10 nm [Q]	140 nm [U]	100 nm [C]
	Demonstrated	590 nm	~1.5 μm [D]	3μm [H]	~700 nm [M]	~2μm [R]	250 nm [V, W]	100 μm [X]
Density (device/cm^2)	Projected	1E10	4.5E9	4.5E9	6E10	1E12	5E9	4.5E9
	Demonstrated	2.8E8	4E7	1E7	2E8	2E7	1.6E9	1E4
Switch Speed	Projected	12 THz	6.3 THz [E]	16 THz [I]	10 THz [M]	1 THz [S]	1 GHz [U]	40 GHz [Y]
	Demonstrated	1 THz	200 MHz [F]	700 GHz [J]	2 THz [N]	100 Hz [R]	30 Hz [V, W]	Not known
Circuit Speed	Projected	61 GHz	61 GHz [C]	61 GHz [C]	1 GHz [L]	1 GHz [Q]	10 MHz [U]	Not known
	Demonstrated	5.6 GHz	220 Hz [G]	10 GHz [Z]	1 MHz [F]	100 Hz [R]	30 Hz [V]	Not known
Switching Energy, J	Projected	3E-18	3E-18	>3E-18	1×10^{-18} [L] [$>1.5\times10^{-17}$] [O]	5E-17 [T]	~1E-17 [V]	3E-18
	Demonstrated	1E-16	1E-11 [G]	1E-13 [K]	8×10^{-17} [P] [$>1.3\times10^{-14}$] [O]	3E-7 [R]	6E-18 [W]	Not known
Binary Throughput, GBit/ns/cm^2	Projected	238	238 [C]	238 [C]	10	1000	5E-2	Not known
	Demonstrated	1.6	1E-8	0.1	2E-4	2E-9	5E-8	Not known
Operational Temperature		RT	RT	4.2 – 300 K	20 K [L]	RT	RT	RT
Materials System		Si	CNT, Si, Ge, III-V, In_2O_3, ZnO, TiO_2, SiC,	III-V Si-Ge	III-V Si	Organic molecules	Ferromagnetic alloys	Si, III-V, complex metals oxides
Research activity [A]			171	88	65	204	25	102

Credit to ITRS'05 report on Emerging Research Devices.

Outline

Carbon


carbon
allotropes
diamond
graphite
carbon nanotube
Fullerene
applications
nanotechnology
Drain
Gate
Source

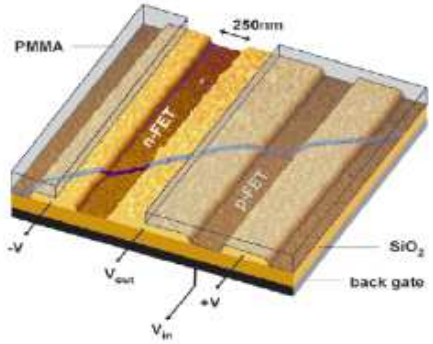
CNT history

Edison's original carbon-filament lamp
US Patent 223898

1880

Discovery of Fullerenes (Smalley)

1985



Carbon nanotube transistor based logic-performing ICs (IBM)

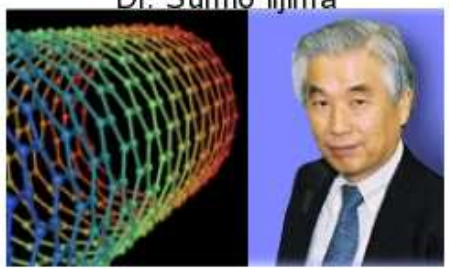
2001

1978

F/A-18 Hornet
The first aircraft with carbon fiber wings

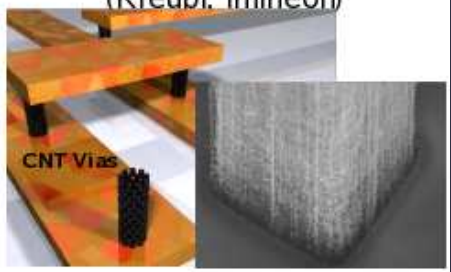
1991

Nanotubes discovered at NEC, by Japanese researcher Dr. Sumio Iijima

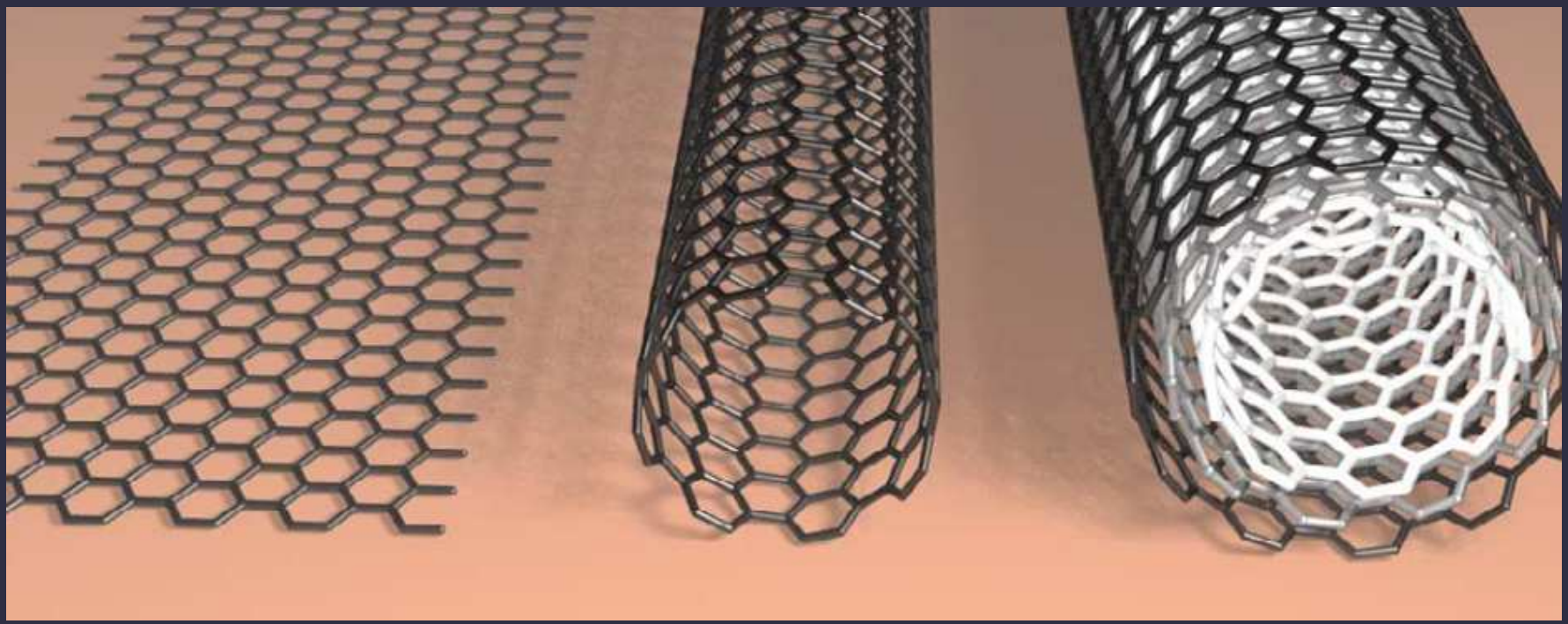


2002

Carbon nanotubes in interconnet applications (Kreupl, Infineon)



CNT classes

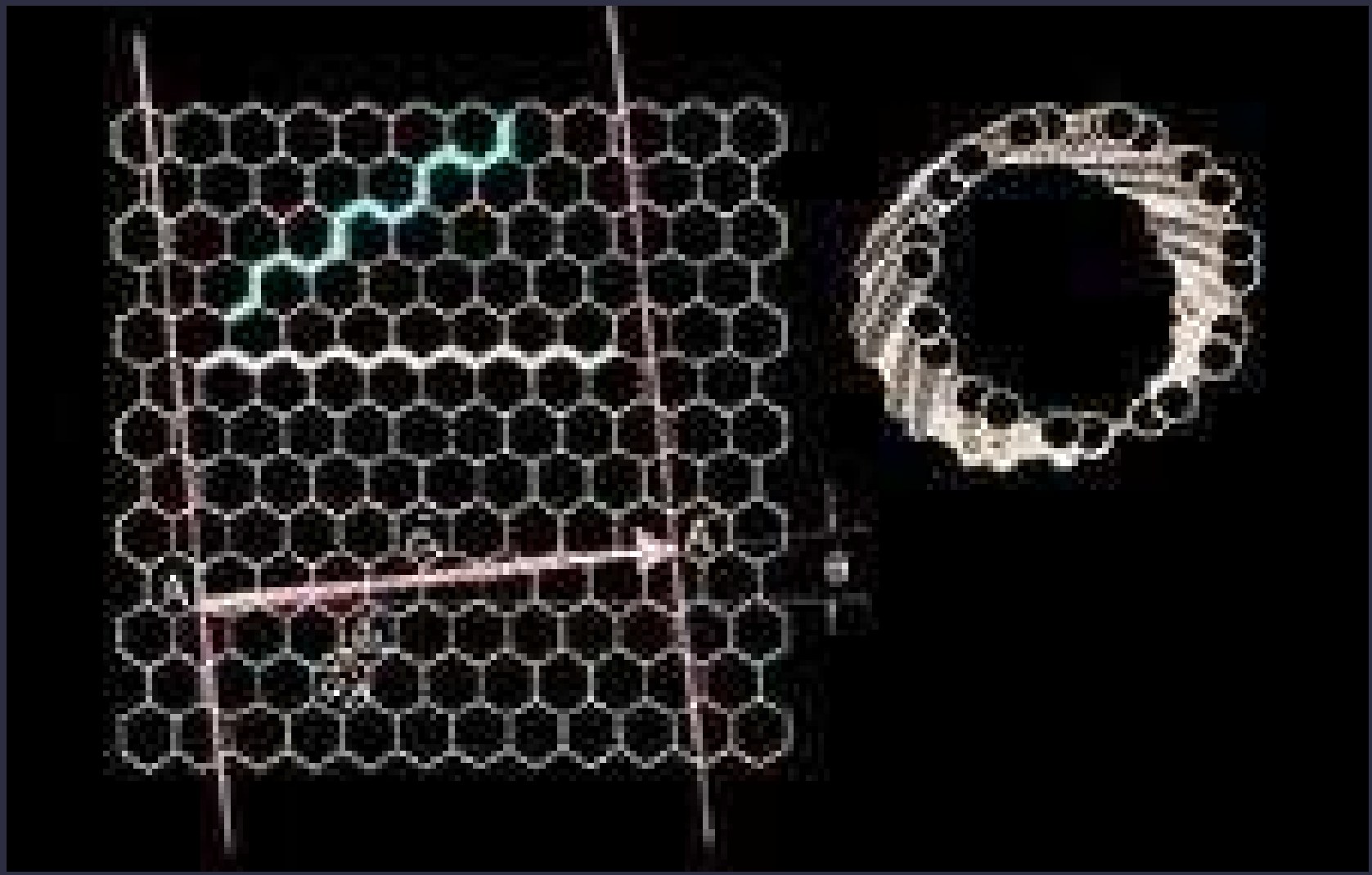


Graphene

Single-walled CNT

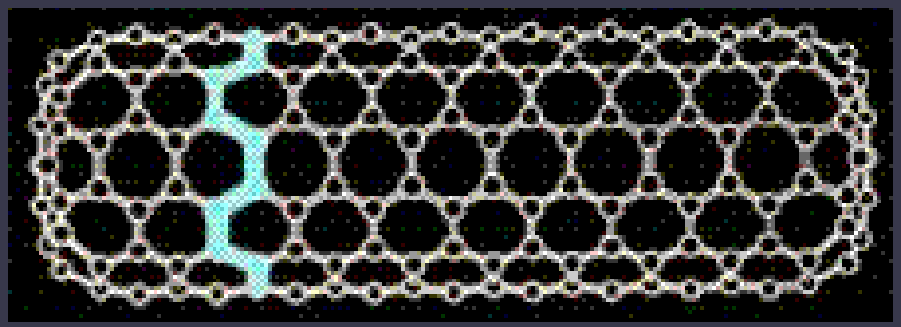
Multi-walled CNT

Chirality

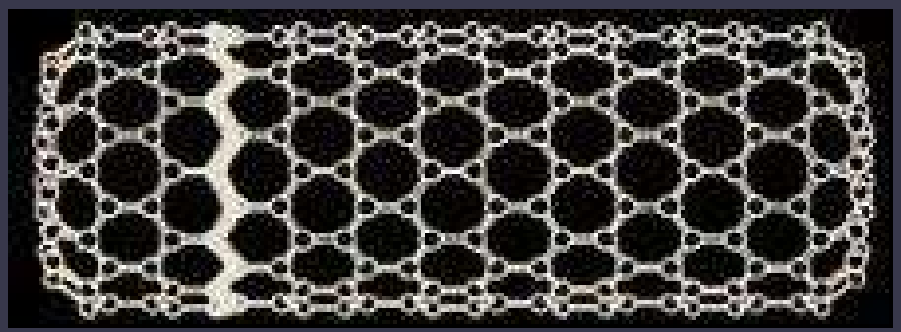


Metallic and semiconducting CNTs

Armchair (metallic)



Zigzag (semi-conducting)



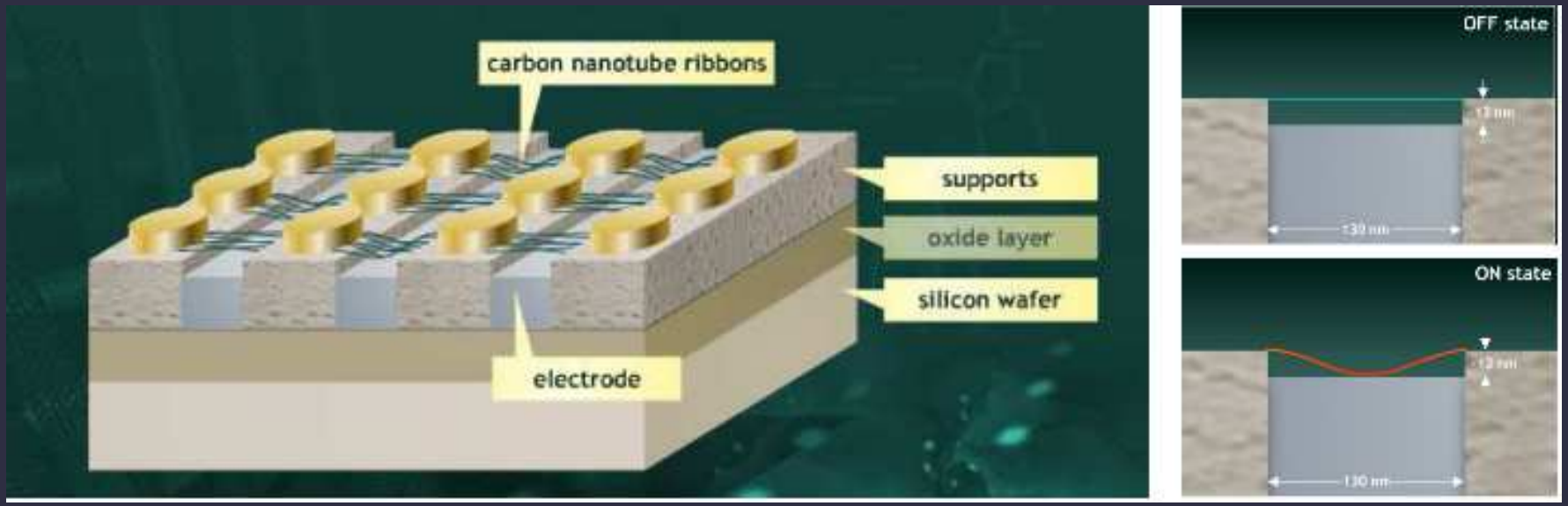
CNT properties

- Metallic or semiconducting.
- Diameter: 0.4–100 nm.
- Length: up to millimeters.
- Ballistic transport.
- Excellent thermal conductivity.
- Very high current density.
- High chemical stability.
- Robust to environment.
- Tensile strength: 45 TPa.
  - Steel is 2 TPa.
- Temperature stability
  - 2,800°C in vacuum.
  - 700°C in air.

CNTs compared with Cu

Property	CNT	Cu
Max I dens. (A/cm^2)	$> 1 \times 10^9$ (Wei et al., APL'01)	1×10^7
Thermal cond. (W/mK)	5,800 (Hone et al., Phy Rev B'99)	385
Mean free path (nm)	$> 1,000$ (McEuen et al. T Nano'02)	40

NRAM

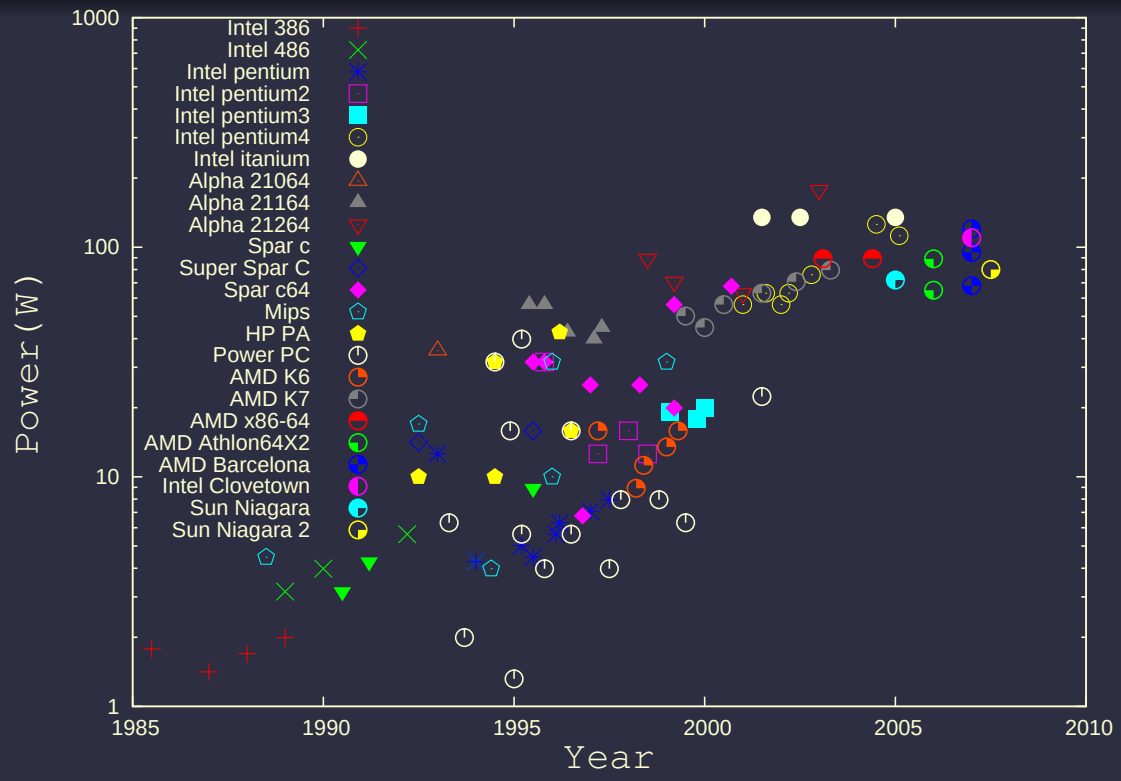


- Uses Van der Waals forces.
- Non-volatile.
- SRAM-like speed.
- DRAM-like density.
- Ready for market in 2007 (and 2008, and 2009, and 2010, and 2011).
- IEEE Spectrum loser of the year. Why?

Outline

Power challenges

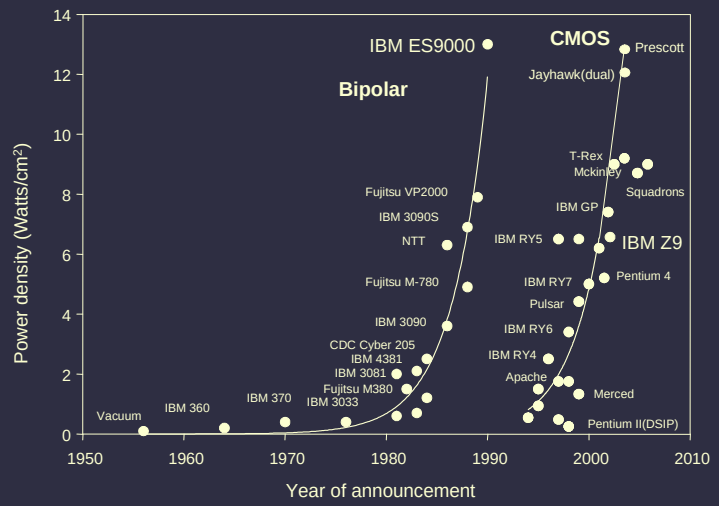
High-performance applications: energy cost, temperature, reliability
Portable embedded systems: battery lifetime



What does history teach us about power consumption?

Device innovations have been the most effective method

- Vacuum tube to semiconductor device in the 1960s
- Bipolar device to CMOS transistor in the 1990s

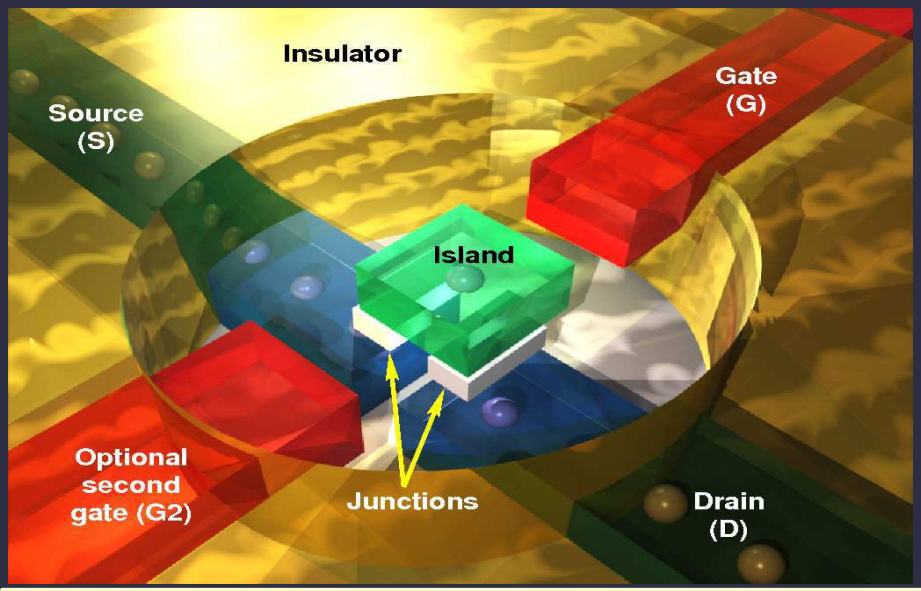


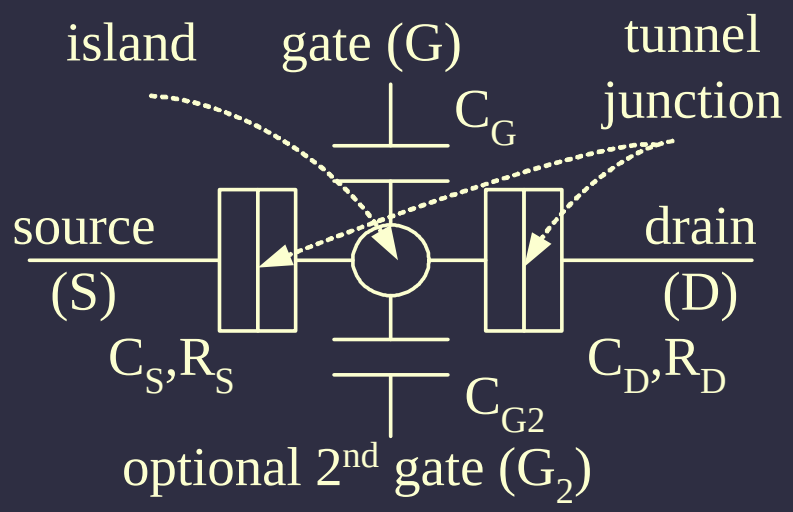
Based on diagram by C. Johnson, IBM Server and Technology Group

Single electron tunneling transistor structure

Device structure

- Island, terminals (source, drain, gate)
- Electron tunneling through tunneling junctions



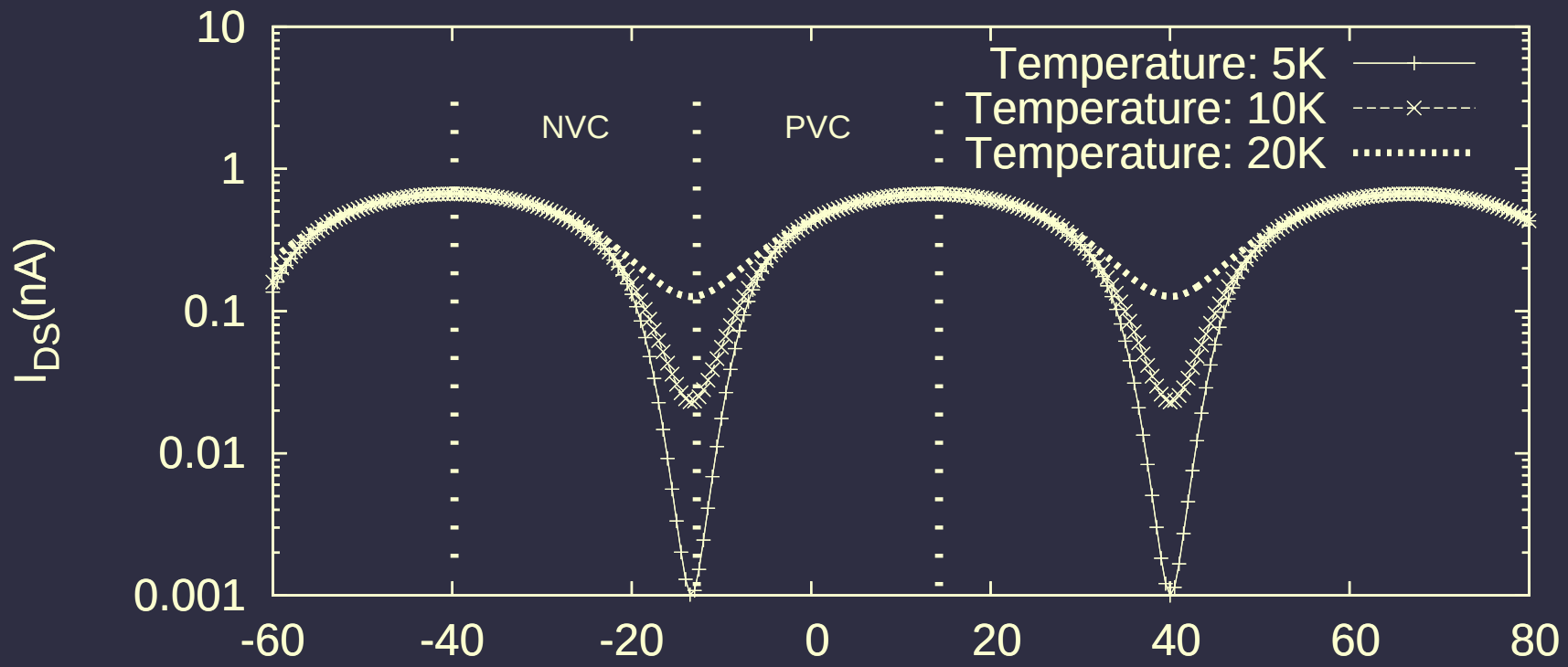


C_G :gate capacitance	C_D :drain tunnel junction capacitance
C_{G2} :optional 2nd gate capacitance	R_S :source tunnel junction resistance
C_S :source tunnel junction capacitance	R_D :drain tunnel junction resistance

Single electron tunneling transistor behavior

Physical principles

- Coulomb charging effect governs electron tunneling
- Coulomb blockade $V_{GS} = me/C_G$, $m = \pm 1/2, \pm 3/2, \cdots$ OFF, $m = 0, \pm 1, \pm 2, \cdots$ ON



SET properties and challenges

Ultra low power

- Projected energy per switching event (1×10^{-18} J)

Room temperature and fabrication challenge

- Electrostatic charging energy must be greater than thermal energy
- $e^2/C_\Sigma > k_B T$
- Requires $e^2/C_\Sigma > 10 k_B T$ or even $e^2/C_\Sigma > 40 k_B T$

SET properties and challenges

Performance challenge

- Electrons must be confined in the island
- $R_S, R_D > h/e^2$, $h/e^2 = 25.8\,\mathrm{k}\Omega$
- High resistance, low driving strength

Reliability concerns

- Tunneling between charge traps cause run-time errors
- Unknown before fabrication
- Device technology: Improved by silicon islands
- Reliable design: Post-fabrication adaptation
- Run-time error correction

Summary

- CMOS will be mainstream for years to come, but not forever.
- The meaning of integrated circuits will change in the future.
- Circuit and logic design fundamentals will still apply.
- Some rules, e.g., difficulty of implementing non linearly separable functions, may change.
- You will each need to adapt as the rules governing device behavior change, but this will be much faster now that you have a foundation.