Henry Ott Consultants

Electromagnetic Compatibility Consulting and Training

Decoupling

Many people today are decoupling digital logic ICs by placing a single 0.1 or 0.01 uF capacitor next to the IC. This is the same method that has been used on digital logic ICs for the last forty plus years, so it still must be the correct approach -- right! After all how much has IC technology changed in the last forty years? I think that it is interesting that this method has worked for as many years as it has. No one should be surprised that, possibly, we are now to the point that a new approach to decoupling is required.

Decoupling is **not** the process of placing a capacitor adjacent to the IC to supply the transient switching current, rather it is the process of placing an L-C network adjacent to the IC to supply the transient switching current. The inductance comes from the capacitor itself (typically 1-2 nH for a SMT capacitor), the interconnecting traces (typically 5 to 20 nH

according to the layout), and the lead frame of the IC (typically 4 to 15 nH according to the type of IC package). From the above we see that the inductance can vary from a low of 10 nH to a high of 37 nH, all assuming a reasonably good layout. It is this inductance that limits the effectiveness of the decoupling network. **It is very important to remember this fact -- we are placing an L-C network between the power and ground, not a capacitor!**

< 50 MHz

Under 50 MHz (don't forget to consider the harmonics of the clock) traditional decoupling methods are effective. Use one or two decoupling capacitors (often 0.1 or 0.01 uF) placed close to the IC power and ground pins. Consider the loop area formed between the decoupling capacitor and the IC, and place the capacitor for minimum loop area.

50 to 500 MHz

Above 50 MHz discrete decoupling capacitors become very inefficient in providing effective decoupling. At these frequencies some form of distributed decoupling capacitance is necessary. This can be achieved by using **many small capacitors** spread out around the IC, or by taking advantage of the **distributed interplane capacitance** between the power and ground planes. The key to using multiple capacitors for high frequency decoupling is to, (1) make them all the same value, and (2) spread them out around the IC --

do not place them together.

The reason that this works is that when equal value L-C networks are placed in parallel, the total capacitance is equal to NxC and the total inductance is L/N where N is the number of capacitors used. In other words, for parallel L-C networks the capacitance value multiples up by the number of networks used and the inductance value divides down by the number of networks used. Both of these effects are working in our favor. For a fixed value of inductance, the effectiveness of the high frequency decoupling network is, therefore, solely dependent on the number of capacitors that you use. The more capacitors the lower the total inductance, and the better the high frequency decoupling. I often recommend from 4 to 20 decoupling capacitors according to the application. Intel, as an example, recommends 41 decoupling capacitors in order effectively decouple a Pentium®-2 microprocessor (Intel Application Note AP-579). When a large number of capacitors are use, there exact placement becomes less important than when only one or two capacitors are used. Just spread them out around the IC, and try to place them symmetrically (or evenly) with respect to the IC.

There are a large number of people that use and/or recommend the use of multiple capacitors of different values. My recommendation is don't! The problem with this approach is that the different value capacitors produce an anti-resonance, or cross-resonance (which produces an impedance peak). Not a desirable result! For those still considering the use of different value capacitors I would suggest that you look at the Bruce Archambeault and Clayton Paul papers referenced below. The Bruce Archambeault

paper in particular gives measured values of decoupling effectiveness, using a network analyzer. For the case of multiple value capacitors it concludes, "There is no noticeable improvement in the high frequency decoupling performance when a second capacitor value is added. In fact the decoupling performance is worse in a frequency range where much of the typical noise energy exists (50-200 MHz)." Archambeault's data shows that the noise increased by 25 dB (as a result of the cross-resonance between the different value capacitors) between 50 and 200 MHz when two different capacitor values were used, as compared to the results when all the capacitors were of the same value.

Although the effectiveness of the decoupling at high frequency is dependent on the number of capacitors used (since the inductance is reduced to L/N), the effectiveness of the decoupling at low frequency has nothing to do with the number of capacitors used. The low frequency decoupling effectiveness is solely dependent upon the value of capacitance (CxN) that all the capacitors add up to. The larger the value of CxN the lower the frequency that the decoupling will still be effective.

If you work out the numbers, you will find that even multiple discrete decoupling capacitors, regardless of how many you use or where you place them, will only be effective up to about 500 MHz.

500 MHz to 5 GHz

Embedded PCB Capacitance: The limit to the concept of

the use of a large number of discrete decoupling capacitors is the use of distributed decoupling capacitance, by taking advantage of the distributed interplane capacitance between the power and ground planes of the PCB. This amounts to an infinite number of infinitesimal capacitors. The only way to get effective decoupling above 500 MHz is to use some form of distributed interplane capacitance. This technique will also be effective down to about 50 MHz. To be effective above 50 MHz a power ground plane capacitance of about 1000 pF/sq. in. is required. Standard layer spacing of 5- to 10-mils provide capacitance that are 1/5 to 1/10 of this required amount.

In 1989-1990 Zycon, (which then became Hadco and now is Sanmina), developed a special PCB laminate with a 2-mil spacing between layers using standard FR-4 epoxy glass as the dielectric. This laminate known as **ZBC-2000** provides 500 pF/ sq. in. of interplane capacitance. By using two sets of power and ground planes in a PCB, we can obtain the desired 1000 pF/sq. in.

Although Zycon has **patents** on the 2-mil thick laminate technology, it is available from many sources. Zycon refers to this technology as **Buried Capacitance**.

This pdf file (~33.5 KB) contains a listing of the printed circuit board fabricators that are licensed to Zycon to manufacture PC boards using this technology. As of 1999, the date of the list, there were 35 printed circuit board fabricators licensed to Zycon to manufacture boards using this technology, and 14 fabricators licensed to produce the special ZBC-2000 laminate.

Although this technology has been available for ten years, it is just now becoming popular. Conversion to a **Buried Capacitance** PCB is very easy, since no new art work is required. Only the layer stack-up is changed. The most common stack-up is as follows:

----------Signal

----------Power*
----------Ground*

----------Signal

----------Signal

----------Ground*
----------Power*

----------Signal

*__Buried Capacitance__ layers

Other layer stack-ups are also possible using the **Buried**

Capacitance approach.

Since no new art work is required, it is very easy to try out this technology by having two sets of prototype boards made, one the standard way and the second using the **Buried Capacitance** layers. Then the performance of the two can be directly compared.

I am convinced that in the future we will all be using some form of distributed capacitance printed circuit boards. They will become the standard way to provide effective decoupling at high-frequency. At the present time the Zycon Buried Capacitanceú technology is the best that is readily available.

> 5 GHz

There is no reason to suspect that the Zycon **Buried Capacitance** technology (or other similar interplane capacitance technology) will not also be effective above 5 GHz, however, I am not aware of anyone who has made any measurements of its performance up at those frequencies.

If you are interested in a more detailed discussion of decoupling and the options available, you might want to consider having our one-day course on **Decoupling and Grounding of High-Speed Digital Circuits** presented at your location.

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References on Decoupling

Paul, Clayton R., **Effectiveness of Multiple Decoupling Capacitors**, IEEE Transactions on EMC, May 1992.

Archambeault, Bruce, **Eliminating the MYTHS About Printed Circuit Board Power/Ground Plane Decoupling**, ITEM 2001.

Sisler, J., **Eliminating Capacitors From Multilayer PCBs**, *Printed Circuit Design*, July 1991.

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