Parasitic Modes on Printed Circuit Boards and Their Effects on EMC and Signal Integrity

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***Abstract*—In this paper, parasitic modes, such as slotline, parallel plane, and surface wave (SW) modes, commonly found on printed circuit boards (PCBs) will be analyzed and their effects on electromagnetic compatibility (EMC) and signal integrity will be discussed. The analysis is based on numerical simulations using the finite difference time domain (FDTD) method which will be shown to be very well suited for rigorous modeling of parasitic mode effects. EMC and signal integrity problems discussed include power loss, crosstalk, ground bounce, and free space radiation. Design guidelines for improved EMC and signal integrity are derived from the results obtained. Comprehensive simulation and characterization of SWs using FDTD is presented for the first time.**

***Index Terms*—EMC, FDTD, parasitic mode conversion, PCB, signal integrity, surface waves.**

I. Introduction

PRINTED circuit boards (PCBs) in modern microelectronics undergo a continuous increase of clock rates and package complexity. Multilayer structures, split reference planes, various interconnects like vias, bends, etc. are common on highly integrated PCBs. In the foreseeable future rules of thumb or simple equivalent circuits will no longer lend themselves to an adequate, comprehensive description of a PCB. The demand for more rigorous, global modeling of the electromagnetic behavior is especially obvious when dealing with spurious or *parasitic modes*. Parasitic modes are electromagnetic modes guided by structures of the PCB that were *not* designed as a waveguide but are nonetheless capable of supporting such modes. The conversion of digital or analog signals into parasitic modes is often termed as *mode conversion* or *mode coupling*. Prominent examples for parasitic mode conversion on PCBs are the excitation of slotline modes on e.g., split reference planes [1]–[8], the excitation of parallel plane modes from e.g., via or flip-chip interconnects [9]–[19], and the excitation of surface wave (SW) modes from, e.g., microstrip discontinuities [20]–[31]. The electromagnetic effects associated with parasitic modes comprise ground bounce, crosstalk, radiation losses, resonance effects and signal degradation in general. Consequently the study of parasitic modes and their effects is a key to understanding and improving electromagnetic compatibility and signal integrity of printed circuit boards.

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In this paper the above mentioned parasitic modes will be analyzed. The analysis is based on numerical simulations using a general purpose finite difference time domain (FDTD) solver [32]. FDTD is nowadays an established method in computational electromagnetics and is well suited for parasitic mode simulation. It dates back to the work of Yee in 1966 [33] and provides a direct solution in the time domain of Maxwell's curl equations for the electric and the magnetic field. The theory is well documented in the literature [34] and excellent text books have been written on the subject [35]–[37]. This paper will demonstrate how the FDTD method is efficiently applied for rigorous modeling and analysis of parasitic modes and their effects on EMC and signal integrity. In Section II slotline modes will be shortly covered to give an introduction to the general effects associated with parasitic modes. In Section III power loss, edge effects, and resonances due to parallel plane modes will be studied in detail. Section IV presents for the first time comprehensive simulation and characterization of SWs using the FDTD method. Throughout the text design guidelines for improved EMC and signal integrity are derived. Finally, conclusions are drawn in Section V.

II. Slotline Modes

In this section a short introduction to the general effects associated with parasitic modes and mode conversion is given using the example of slotline modes. Parasitic slotline modes are typically excited on microstrips crossing split power or ground planes. Splitting of ground and/or power planes may be necessary in PCB and MCM design if, e.g., a separation of noisy digital logic from sensitive analog circuitry or the introduction of different voltage reference areas is desired. Slotline mode characteristics and microstrip to slotline mode transitions have been studied in detail in the literature [1]–[8]. FDTD simulations of slotlines are presented, e.g., in [6]. Parasitic slotline mode conversion in general is discussed in [8].

A. Parasitic Mode Conversion Process

As an introduction, consider Fig. 1 where FDTD results are shown for a Gaussian pulse propagating on a microstrip that crosses a split ground plane (400-μm wide microstrip on 200-μm FR4 substrate and perfect electrically conducting ground plane, gap width 200 μm.). The gap in the ground plane forms a slotline mode waveguide. The snapshot of the absolute electric field strength shows four distinct pulses: the forward and backward scattered pulses on the microstrips (contributing mainly to the z-component of the electric field) and the two excited pulses on the slotline (contributing mainly to the y-component of the electric field).

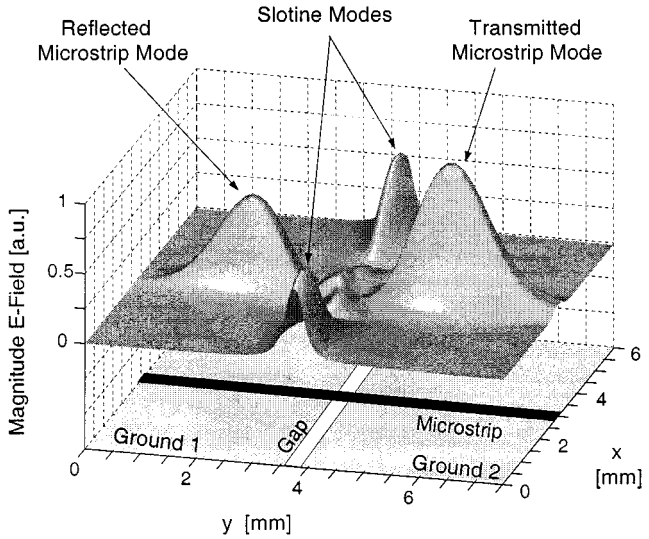

Fig. 1. Identification of slotline mode excitation from a microstrip split plane crossing by FDTD simulation. Snapshot of the absolute electric field strength at medium substrate height (geometry below electric field map).

According to [8] the excitation of slotline modes can be described using the displacement current (and its according electric field) flowing onto the second ground plane. That is the pulse charges traveling on the microstrip and the pulse charges traveling on the first ground plane will induce charges of opposite sign but equal amount on the second part of the ground plane. One part of the induced charge will then pair with charge on the microstrip and thus allow transmission of the pulse. The other part will pair with charge on the first ground plane and thus constitute the parasitic slotline mode. The remaining charge on microstrip and first ground plane will convert into pulse reflection.

Of course such an explanation is not able to explain the frequency dependence or amount of power losses of the mode conversion process but it reflects correctly the general correlation between the displacement current flowing between the two planes and the conduction current flowing in the microstrip: the more charge is induced the more charge will be transmitted.

B. Parasitic Mode Conversion Effects

In order to avoid crossing of split planes isolation transformers, optical isolators, or metalized bridges are typically used in practice. However, design constraints may not always allow these solutions. In this case it is necessary to study the associated electromagnetic effects.

Fig. 2 attempts to give an overview of the most important phenomena: Consider a digital or analog signal propagating on a transmission line (denoted by Z_0). When the signal reaches a discontinuity like a gap in the ground plane, part of its energy will be converted into a mode traveling on a parasitic waveguide (denoted by Z_p). This conversion process will be accompanied by power loss, reflection, and degradation of the transmitted signal. The parasitic mode itself can couple into other transmission line modes thus causing crosstalk noise, or it can be reflected by e.g., the PCB edges thus causing free space radiation and resonance effects. Not shown in Fig. 2 is the potential coupling of different parasitic modes with each other like slotline mode to parallel plane mode conversion.

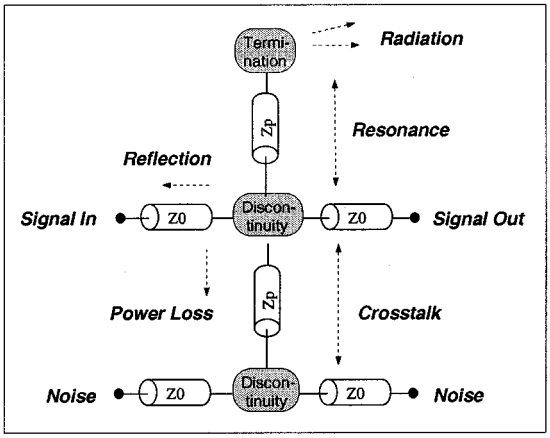

Fig. 2. Schematic overview of the most important electromagnetic effects associated with parasitic modes on PCBs (Z_0 denotes normal waveguides, Z_p parasitic modes).

In summary, the effects associated with parasitic mode conversion include reflection, power loss, signal degradation, crosstalk, resonance and free-space radiation, all of which are serious problems for EMC and signal integrity.

III. Parallel Plane Modes

Parasitic parallel plane mode excitation finds more and more interest in research and development (see, e.g., [11]–[13]). FDTD simulations were presented in [10], [14], [15], and [19]. In [16] the FDFD method was used. In this section some new FDTD results for parasitic parallel plane modes will be presented which complement the available literature on the subject. For background information, the reader is referred to [9].

A. Excitation and Propagation Characteristics

Consider a two-layer PCB made out of a homogeneous and isotropic dielectric substrate. Under the assumption that both substrate and conductors show only negligible losses one finds that at all frequencies TEM waves can propagate in the space between the planes with a velocity of $v_{\rm ph} = 1/\sqrt{\mu\varepsilon}$ and a wave impedance of $\eta_0 = \sqrt{\mu/\varepsilon}$. The next higher modes (TE and TM, respectively) have cutoff frequencies of [9]

$$f_n = n \cdot \frac{v_{\rm ph}}{2h}, \qquad n = 1, 2, 3, \ldots$$

where h is the distance between the planes (in all cases considered here the excitation bandwidth of FDTD simulations was kept below the cutoff f_1).

However, on PCBs parasitic parallel plane (pp) modes will in general be excited at the point-like locus where a signal waveguide crosses at least one of the planes. From this locus the pp-modes will propagate radially away with completely changed behavior of the wave impedance and with decreasing amplitude. As an example consider the generic FDTD model of a via interconnect on a double-layer PCB (Fig. 3). The signal carrying microstrip line jumps from the top of the PCB to the middle by crossing the power plane through the via hole. This discontinuity in the signal trace leads to reflections, degraded signal transmission and excitation of parasitic parallel plane modes. To prove the last point the structure of Fig. 3 was simulated

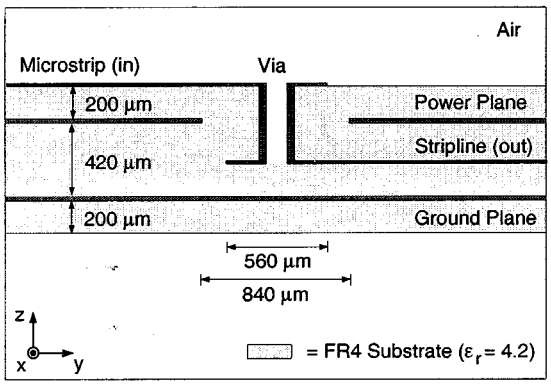

Fig. 3. Generic FDTD model of a via interconnect on a double-layer PCB. Conductors are perfect with a thickness of 20 μm, microstrip and stripline width are 400 μm. Impedance of the microstrip was approximately 48 Ω, impedance of the stripline was approximately 35 Ω.

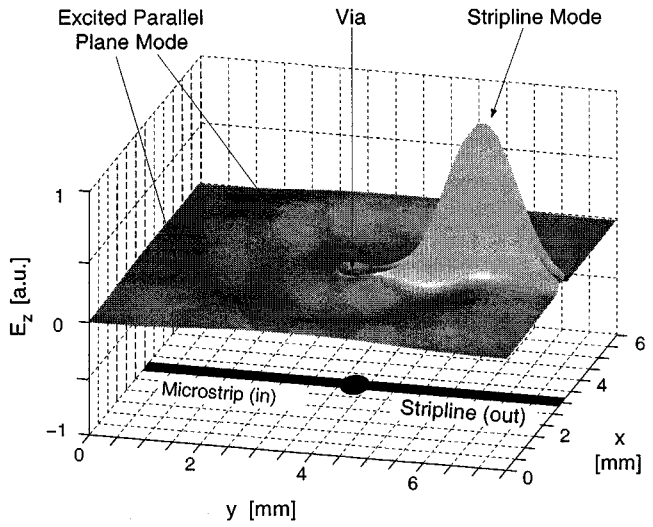

Fig. 4. Identification of parallel plane mode excitation from the via of Fig. 3. Snapshot of the vertical electric field components just above the stripline (geometry below electric field map). The parallel plane mode amplitude reaches about 4% of the stripline mode amplitude.

with FDTD using a Gaussian pulse excitation at the beginning of the microstrip and recording of its propagation on the via. Minimum grid spacing was 20 μm, stable time step was approx. 0.039 ps and total simulation time was 0.25 ns. Fig. 4 shows the FDTD result: a snapshot of the z-component of the electric field in a layer in between power and ground plane at the time of pulse scattering. Two modes can be distinguished here: First, the (dominant) stripline mode on the right side of the model. Second, the smaller, circular wave front of the pp-mode propagating radially away from the via. It can be shown analytically that the according wave impedance is radially dependent on the distance r to its origin [9]

$$\eta_{\mathrm{pp}}(\beta r) = \frac{E_z(\beta r)}{H_\varphi(\beta r)} = \frac{\eta_0}{\sqrt{\varepsilon}} \cdot \left| \frac{H_0^{(1)}(\beta r)}{H_1^{(1)}(\beta r)} \right|$$

where the triple (r, z, φ) refers to cylindrical coordinates and where $H_0^{(1)}(\cdot\cdot)$ and $H_1^{(1)}(\cdot\cdot)$ are Hankel functions of the first kind and of order 0 and 1, respectively. The wave impedance $\eta_{\mathrm{pp}}(\beta r)$ is a monotonically increasing function tending toward zero for small arguments and toward η_0 for large arguments. The Poynting vector will decrease proportional to $1/r$ according to power conservation in a cylindrical geometry. These properties can be extracted from FDTD simulations as has been shown in [19].

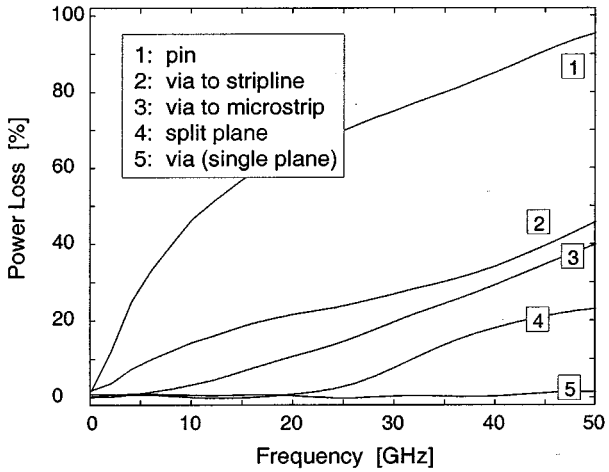

Fig. 5. Power loss due to parasitc mode conversion for different structures. Loss was calculated using (1) after scattering parameter extraction from FDTD data.

B. Power Loss

The pp-mode conversion process at the via location will be accompanied by considerable power loss. Power loss of linear two-port systems can easily be calculated from FDTD simulations by extracting the scattering parameters of the structure and calculating

$$\text{Power Loss} = 1 - |S_{11}|^2 - |S_{21}|^2 \qquad (1)$$

where port 1 corresponds to the input and port 2 to the output. The scattering parameters in the frequency domain are usually obtained after Fourier transformation of wide-band Gaussian pulse excitation in the time domain.

Fig. 5 shows results gained from FDTD simulations of different structures (substrate and conductors were modeled lossless). For all structures the input port was the microstrip of Fig. 3 whereas the remaining geometry was:

- a pin (board as in Fig. 3 but with via connected to ground);
- a stripline (as in Fig. 3);
- a microstrip (board as in Fig. 3 but with via crossing both layers and connected to a second microstrip);
- a split plane (single layer board, gap width 200 μm, gap length 28.2 mm);
- a single-plane via (connected to a second microstrip).

The most dominant power loss is exhibited by the pin structure. This indicates that package ground pins are very good emitters of pp-modes causing what is called ground bounce or simultaneous switching noise. Next come the double-layer via structures. In [19] it was shown by FDTD simulations that increasing the capacitive coupling between power and ground plane (e.g., by reducing plane to plane distance or adding bypass capacitors) will improve the transmission properties of double-layer vias. Beside the capacitance value the location of the bypass capacitors has a major impact on the coupling between the two planes. The nearer the capacitors are placed to the via and the more they cover the pp-mode wave front the better the coupling and hence the via transmission. The split plane structure is depicted

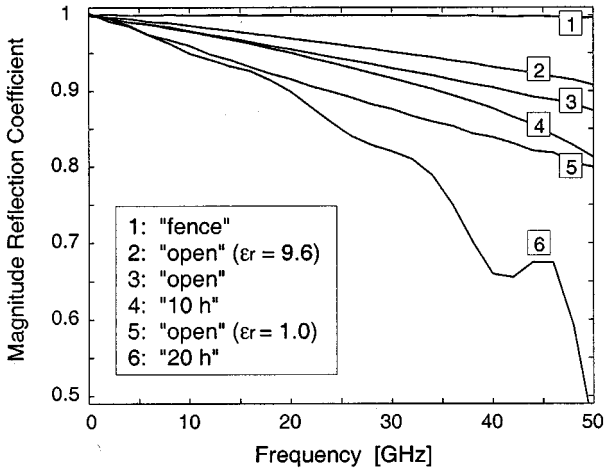

Fig. 6. Reflection coefficient for different PCB edge configurations gained from FDTD data after Fourier transformation (plane-to-plane distance $h = 420\ \mu$m, dielectric constant of substrate $= 4.2$ if not stated explicitly, dielectric constant of surrounding air $= 1.0$).

for reference showing loss due to slotline mode conversion. Finally comes the single-layer via showing negligible losses. For all structures loss increases with frequencies.

From what was found, design guidelines for improved EMC and signal integrity can be derived. 1) Vias should be avoided whenever possible on multilayer boards. Vias on single-layer boards are much less critical. 2) Good cpacitive coupling should be provided between all reference planes. 3) Microstrip to stripline vias should be preferred instead of using microstrip to microstrip vias, i.e., as few reference planes as possible should be crossed. 4) High-frequency signals should be routed on one and the same layer.

C. Edge Effects

The injected pp-modes will sooner or later impinge on the PCB edges which terminate their propagation. Part of the energy will be reflected and part of it will be radiated into free space both of which effects represent problems for EMC and signal integrity. Here FDTD was used to analyze reflected and radiated power for different edge geometries found in PCB design. More precisely, the edge geometries studied were:

- "open", i.e., aligned truncation of planes and dielectric substrate (with varying substrate permittivity from 9.6 to 4.2 and 1.0);
- "fence", i.e., additional connecting via between the planes (diameter approx. 400 μm);
- "Xh", i.e., one plane cut back by X times the distance h between the planes ($X = 10$ and 20).

Figs. 6–8 show FDTD results in terms of reflection coefficients, electric near- and far-field plots.

For extraction of the reflection coefficients and near-fields the FDTD model was designed quasi two-dimensional which could be achieved by using perfectly magnetic conducting (PMC) boundary conditions in the xy-plane. Thus the number of grid cells could be reduced to one for the open and Xh edges and to eight for the fence edge. The distance between the two planes was kept at 420 μm. Minimum grid spacing was 20 μm and stable time step was about 0.066 ps. For excitation a plane wave was injected between the two planes using a wide-band

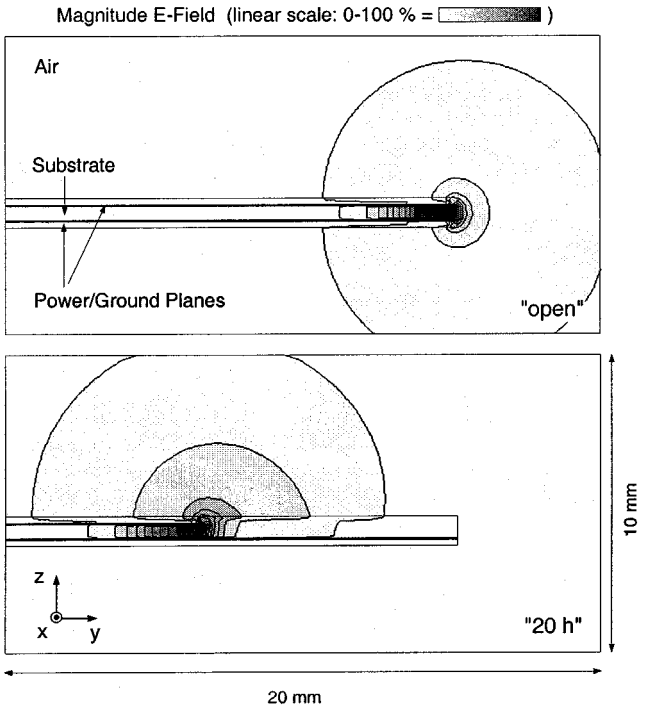

Fig. 7. Snapshot of the absolute electric field strength at the moment of pulse reflection for the open PCB edge and the $20h$ PCB edge (power plane cut back by $20 \times h$, where h is the plane-to-plane distance of 420 μm).

Gaussian pulse modulation. From time domain voltage data the reflection coefficient could be extracted in the frequency domain after Fourier transformation.

As can be seen, all edge geometries are highly reflective for low frequencies (reflection >98% below 5 GHz). In this range the parallel planes form a resonator of very high Q (see below). At higher frequencies the differences between the edge geometries become apparent. Obviously the fence edge acts more or less like a shorted end, reflecting nearly all energy. In contrast the $20h$ edge shows considerable radiation losses. In between are the $10h$ edge and the open edges. It is interesting to see that the closer the substrate permittivity and the surrounding air permittivity match the more energy will get radiated. Fig. 7 shows snapshots of the electric near fields of the open edge and the $20h$ edge at the moment of pulse reflection. Even if it is difficult to see here quantitative differences it is obvious that there is a completely changed radiation pattern. This may become important for correct placement of sensitive components nearby the PCB edges.

The near-field differences translate themselves into according far-field patterns. In order to extract the far-fields simplified FDTD models of a complete 10×20-cm PCB embedded in air with $h = 1$ mm were generated and exited by a single harmonic excitation of 1 GHz. Minimum grid spacing was 1 mm, stable time step was about 1.926 ps and total simulation time was 10 ns. Fig. 8 shows the normalized electric far-field amplitudes of the open and $20h$ board in the yz-plane. As supposed the $20h$-board shows increased radiation and strong orientation toward the top of the PCB. Hence the $20h$-board may be no good choice if sensitive components are placed nearby.

Coming back to the reflected power, one encounters EMC and signal integrity problems, too. As indicated before, the high reflectivity of e.g., the open board edges leads to multiple reflec-

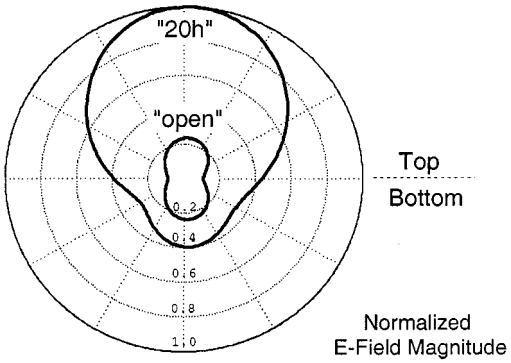

Fig. 8. Far-field radiation pattern at 1 GHz of complete 10×20 cm PCBs in air (models were simplified with a plane-to-plane distance of $h = 1$ mm). As indicated by Fig. 7 the $20h$ PCB radiates more energy and has a strong orientation toward the top.

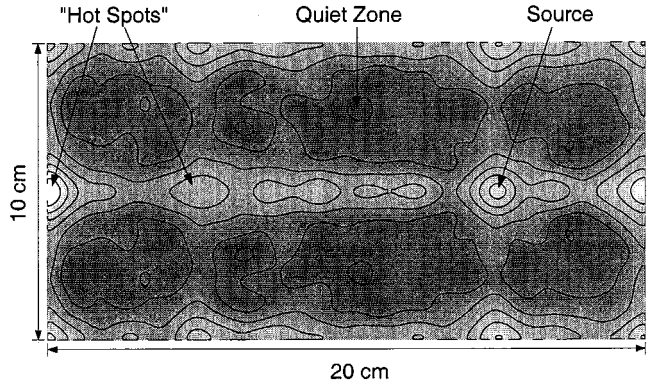

Fig. 9. Electric field fluctuations on 10×20-cm double-layer PCB (plane-to-plane distance $h = 1$ mm, dielectric constant $\varepsilon_r = 4.2$). The fluctuations were calculated by sampling the vertical electrical field components between power and ground plane over 90 ns every single ns (dark gray = small fluctuations, light gray = high fluctuations).

tions of pp-modes. Eventually the original radial behavior of these modes is lost and a rather "chaotic" fluctuation of the voltage between the two planes will result. Transferring this result into the frequency domain, one can state that the pair plane forms a resonator of considerable high Q [15], at least for the frequencies considered here. If one approximates the plane edges as perfect open ends the resonance frequencies for parallel plane modes follow to

$$f_{nm} = \frac{c_0}{2\sqrt{\varepsilon_r}} \cdot \sqrt{\left(\frac{n}{L_x}\right)^2 + \left(\frac{m}{L_y}\right)^2}, \qquad n, m = 0, 1, 2, \ldots$$

where $L_{..}$ are the lengths of the edges in x- and y-dimension, respectively. In [19] these resonances could be confirmed by FDTD simulations. As an example consider Fig. 9 where a field map of the noise between power and ground plane of the 10×20 cm PCB has been extracted from FDTD simulation. After having injected a wide-band Gaussian pulse in between the planes the electric field deviations over 90 ns were recorded and averaged corresponding to

$$E_{z,\text{fluct.}}(x, y) = \sqrt{\frac{1}{91} \cdot \sum_{i=0}^{90} E_z(x, y, t_i)^2}$$

where $t_i = 10\,\text{ns} + i \cdot 1\,\text{ns}$. On real PCBs the pair of planes contains many sorts of vias, chip pins and other discontinuities changing the resonance behavior. FDTD is well suited to simulate such configurations. Results may be useful for placing and dimensioning bypass capacitors and the detection of "hot spots" or "quiet zones" where voltage fluctuations are maximal or minimal, respectively.

Concerning EMC and signal integrity on multilayer boards, one finds in summary that: 1) energy injected into the space between parallel planes causes both ground bounce noise and free space radiation; 2) any pair of parallel planes forms a resonator of considerable high Q; 3) not all areas of a parallel plane resonator show the same noise. There are "hot spots" as well as "quiet zones"; 4) free-space radiation from board edges increases with frequency; 5) amount and directivity of free space radiation depend on the edge geometry.

Consequently, the amount of energy injected into the parallel planes has to be kept as small as possible. Further suggestions to reduce EMC and signal integrity problems are, e.g., a dissipative edge termination [17] or electronic bandgap structures for the substrate [18].

IV. Surface Wave Modes

Grounded dielectric planes like PCB surfaces are capable of supporting propagating waves. The supported modes are called *trapped modes* (referring to their nonradiating nature), *slow-wave modes* (referring to their phase velocity less than that of light in vacuum) or *SW-modes* (referring to their exponential decay perpendicular to the surface). Parasitic SW-mode conversion occurs essentially on microstrip structures. Their excitation has been studied, e.g., by [22]–[24], their relation to free space radiation was subject of [25]–[27], and their potential for crosstalk was described in [28]. First FDTD results have been presented in [29], but it has been shown in [30] for the first time how FDTD may be used to predict dispersion, wave impedance, scattering behavior, excitation and interference of SWs. The knowledge of these fundamental properties is essential if one wishes to optimize the electrical performance of packages and interconnects with respect to SW crosstalk and radiation losses. Analytic results for SWs can be found, e.g., in [20] and [21].

A. Extraction of Mode Characteristics

In PCB and antenna design the fundamental transverse magnetic (TM_0) SW-mode is of primary interest since it has zero cutoff and may be present at all frequencies. The next higher sw-mode is the fundamental transverse electric (TE_1) mode with a cutoff frequency usually in the high GHz range. In general the cutoff frequencies f_n of TM_n $(n = 0, 2, 4, \ldots)$ and TE_n $(n = 1, 3, 5, \ldots)$ SW-modes on a grounded, lossless dielectric substrate of height h and relative permittivity ε_r can be calculated by [29]

$$f_n = n \cdot \frac{c_0}{4h \cdot \sqrt{\varepsilon_r - 1}}.$$

Both TM_0 and TE_1 mode show strong dispersive behavior which can be extracted from FDTD simulation by using the relations

$$\eta_{\text{TM}} = -\frac{E_z}{H_x} = \frac{\beta_{\text{TM}}}{\omega\epsilon} \quad \text{and} \quad \eta_{\text{TE}} = \frac{E_x}{H_z} = \frac{\omega\mu_0}{\beta_{\text{TE}}} \qquad (2)$$

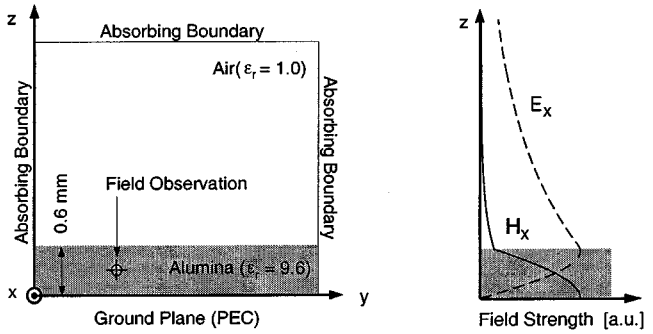

Fig. 10. FDTD model of a grounded, lossless dielectric plane (left). Analytical transverse field strengths at 50 GHz for the TM_0 (solid line) and the TE_1 (dashed line) SW-mode after [21] (right).

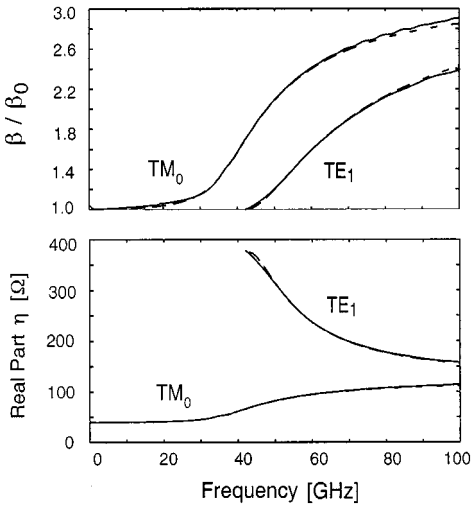

Fig. 11. Comparison of FDTD results (solid lines) with analytical results (dashed line) after [21]: Dispersion characteristics (top). Wave impedances in the substrate (bottom). Note that Z_{TM} in the air is by a factor $\varepsilon_r = 9.6$ higher.

where $\eta_{..}$ denote the wave impedances and $\beta_{..}$ denote the phase constants of TM and TE modes, respectively.

Fig. 10 shows an FDTD model suitable for sw-mode analysis. The FDTD model was uniformly spaced with 60 μm and consisted of 1000 cells in y-dimension and 110 cells in z-dimension. In x-dimension the extent of the structure was assumed to be infinite. This could be accounted for by using perfectly magnetic conducting (PMC) boundaries for the TM case and perfectly electric conducting (PEC) boundaries for the TE case which allowed to reduce the number of cells to one in this dimension. The cutoff frequency for the TE_1 mode in this model was about 42.6 GHz. For excitation the E_z field components in the TM case and the E_x field components in the TE case were used over the whole cross section of the computational domain. The fields were recorded at medium substrate height 500 cells away from the excitation. The stable time step was about 0.116 ps and total simulation time was 1 ns.

Fig. 11 shows FDTD results for wide-band Gaussian pulse excitation. After Fourier transformation the frequency domain phase constants and wave impedances could be extracted using Eqs. (2). Both show good agreement with analytical values from [21]. Figs 12 and 13 shows FDTD results for single harmonic excitation. In Fig. 12 the phase offset between electric

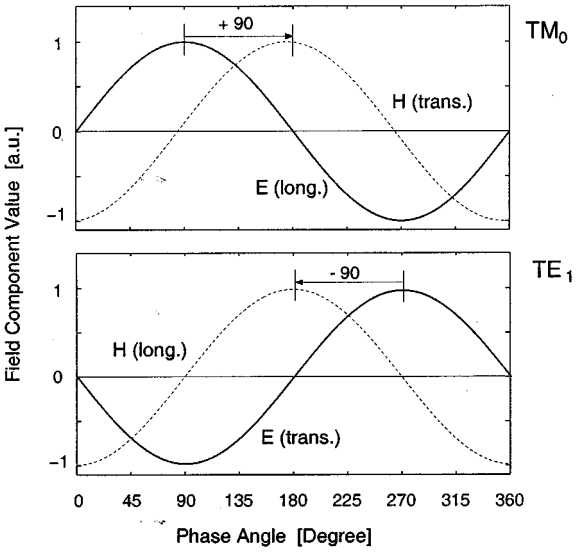

Fig. 12. FDTD results for surface impedance of TM_0 (top) and TE_1 (bottom) SW-modes from FDTD simulation at 50 GHz (single harmonic excitation). As predicted by analytical calculations [20], the TM_0 mode shows inductive behavior whereas the TE_1 shows capacitive behavior.

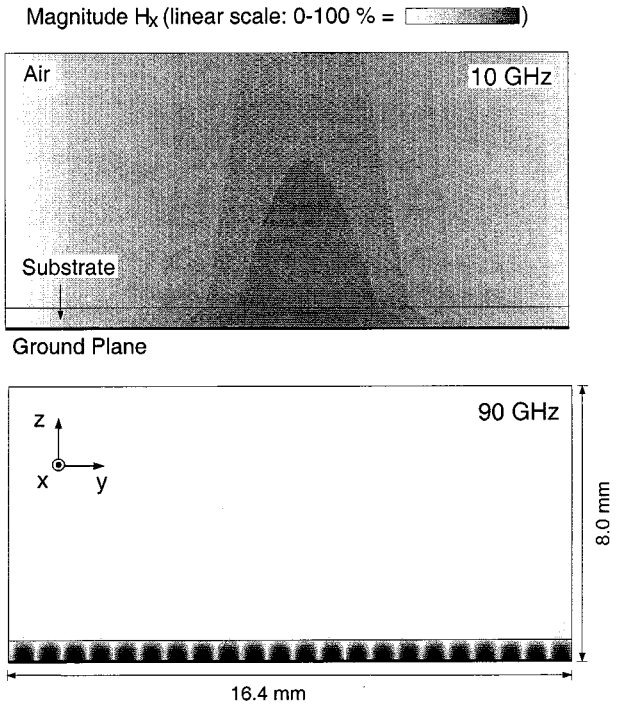

Fig. 13. Snapshot of the transverse magnetic field H_x of the TM_0 SW-mode for different frequencies (harmonic excitation). At 10 GHz the mode is "quasi plane wave" whereas for 90 GHz the mode seems to be "trapped" near the surface.

and magnetic components looking *down* on the surface are depicted. It can be seen that for both TM_0 and TE_1 the surface impedance is purely reactive, i.e., inductive for the TM_0, and capacitive for the TE_1 mode. Again, this is in perfect agreement with analytical results [20]. Finally, in Fig. 13 time domain snapshots of the transverse magnetic field H_x show the different lateral extensions of the TM_0 SW-mode for different frequencies. The field plot confirm the analytical result that the TM_0 sw-mode behaves essentially like a plane wave for fre-

quencies approaching zero whereas for high frequencies the influence of the substrate becomes dominant and the mode is "trapped" near the surface [21]. Concerning EMC and signal integrity issues FDTD showed that this "trapped" version bears most of the problems (see below).

B. Excitation and Crosstalk

The excitation of SWs from microstrip discontinuities is a well-known high frequency effect on PCBs. Fig. 14 show FDTD results for three different microstrip geometries: an open end, a right angle bend, and a T-junction. All microstrips were 0.6 mm wide and the substrate was the same as in the model of Fig. 10 ($h = 6$ mm, $\varepsilon_r = 9.6$). A wide-band Gaussian pulse was injected on each microstrip and the vertical electric field strength was recorded at medium substrate height in order to detect SWs excitation from the discontinuity. Obviously all structures excite SWs (mainly in forward direction) spreading out on the ground plane.

Fig.15 refer to a simulation where a second right angle bend was placed 3.6 mm away from the first one with microstrips oriented in opposite directions ("mirrored geometry"). The voltage measured below the second bend reveals the amount of crosstalk on the second microstrip produced by electromagnetic interference (the crosstalk amplitude reaches about 20% of the transmitted pulse amplitude). The corresponding scattering parameters reveal that crosstalk sets in significantly at about 40 GHz. It can be shown analytically that below this frequency most of the energy is propagating within the air and above most of it is propagating in the substrate [21]. Hence one may conclude that indeed radiation of SWs, and not capacitive coupling, is the important electromagnetic interference mechanism here. Concerning improvement of EMC and signal integrity, first means to reduce crosstalk would be to place the second bend further apart or out of the main direction of SW propagation.

C. Edge Effects

In reality SWs are propagating on a finite size plane which may be terminated e.g., by a dielectric truncation or a dielectric and ground plane truncation. Similar to pp-modes, SW-modes will will be partly scattered back and partly radiated from these truncations. Especially the spurious free-space radiation has found attention in the study of printed circuit antenna performance [23], [26]. Fig. 16 shows FDTD results of TM_0 backscattering for two different edge geometries. The reflection coefficients were obtained by taking the ratio of the Fourier transforms of incident and reflected TM_0 SWs. The FDTD model parameters were equal to those already described except that the computational domain was enlarged in order to allow free-space radiation. Both coefficients show a clear increase in reflection at about 40 GHz. As stated before, above this frequency most of the SW-mode energy is propagating in the substrate. As stated too, it was found that the TM_0 SW-mode behaves essentially like a plane wave for small frequencies whereas for high frequencies the mode is trapped near the surface. Hence it appear plausible that a change in the reflection coefficient occurs where the SW-mode changes its behavior from "quasi-plane-wave" to "trapped".

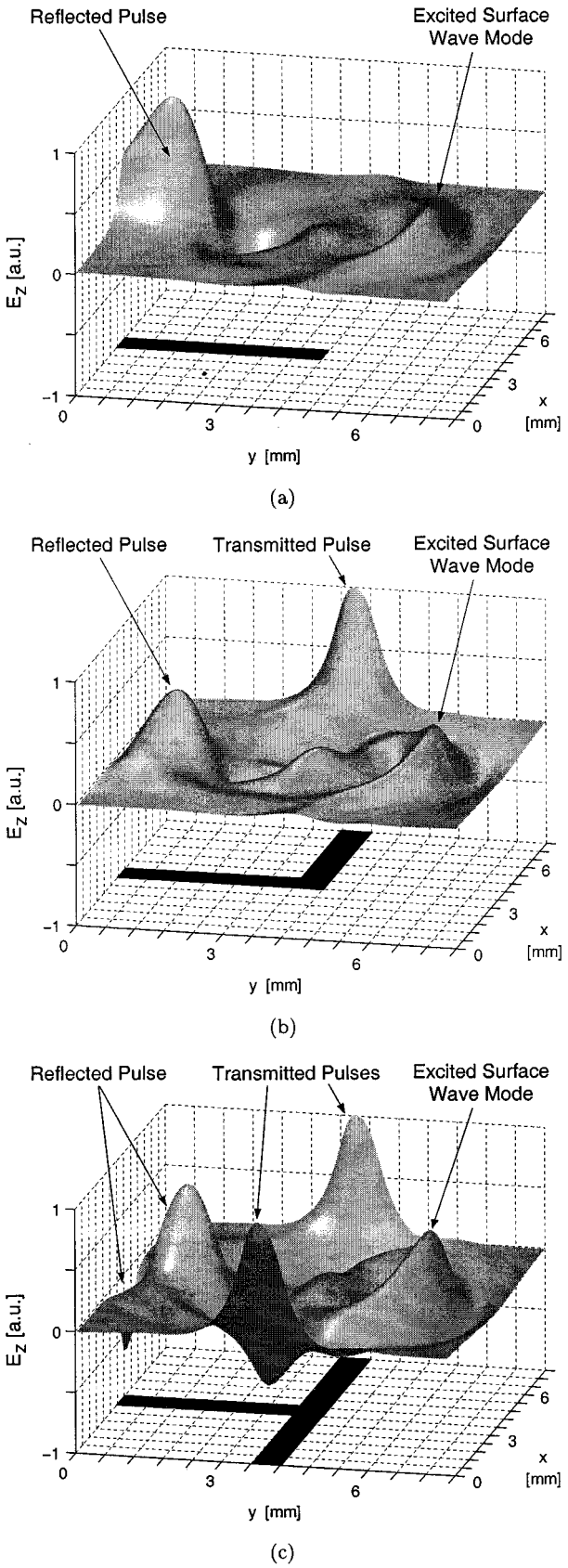

Fig. 14. Identification of SW excitation from microstrip structures by FDTD simulation: (a) open end, (b) right angle bend, (c) T-junction. Snapshot of the vertical electric field strength at medium substrate height (geometry below electric field map, all amplitudes normalized to the same value). Clearly all structures show SW-modes spreading out into the forward direction.

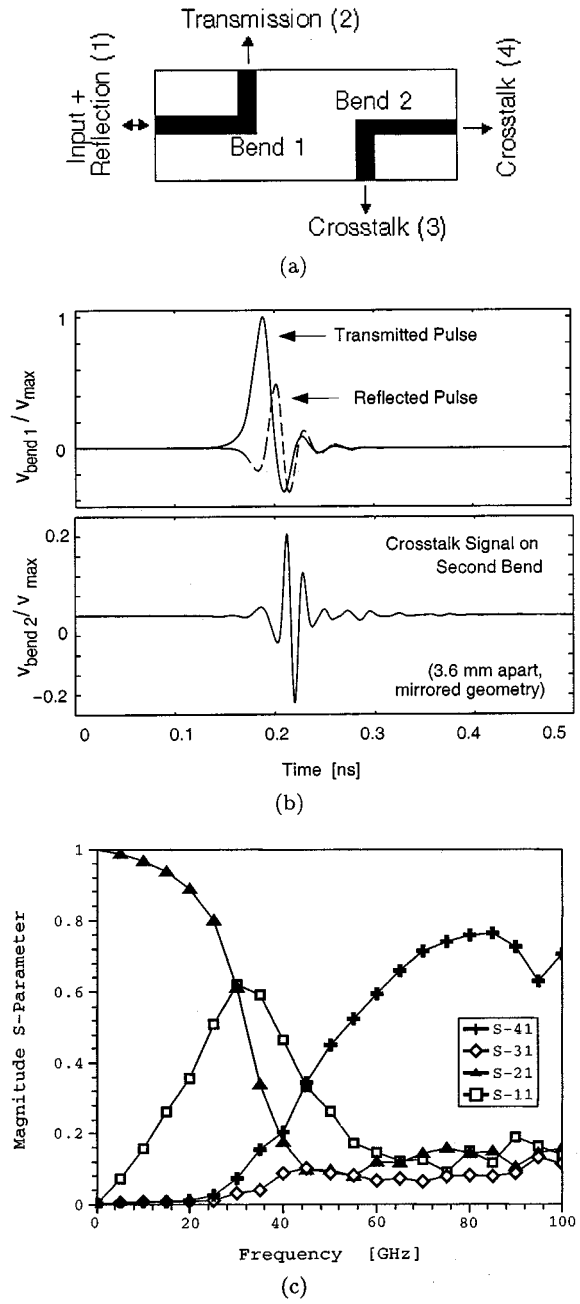

Fig. 15. FDTD analysis of crosstalk due to SWs on two right angle bends: (a) Placement of the bends and port numbering (bends are 0.6 mm wide and 3.6 mm apart). (b) Normalized voltage curves on the first microstrip bend (top) and the second bend (bottom). The crosstalk amplitude reaches about 20% of the transmitted signal maximum. (c) Scattering parameters extracted from time domain data. Crosstalk increases significantly above 40 GHz (see text).

For low frequencies the reflection coefficient for the dielectric truncation (geometry I) approaches zero as expected whereas the reflection coefficient of the dielectric and ground plane truncation (geometry II) notably does not approach one. This might be due to FDTD specific problems of properly exciting the SW at low frequencies. However, the existence of a weak plane wave could be observed propagating on the lower side of the ground plane (Fig. 16) indicating that this geometry is not an "open end" for this kind of SW simulation. Further investigations might be necessary here.

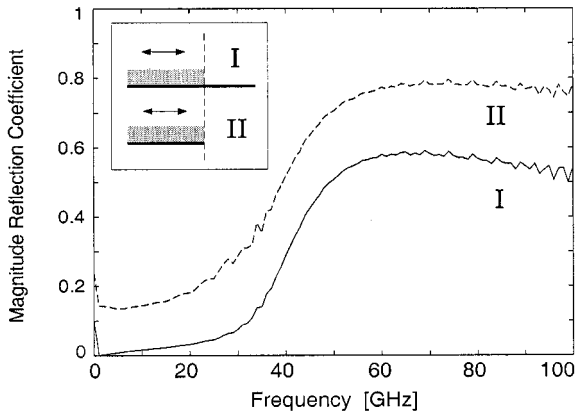

Fig. 16. Reflection coefficients of TM_0 SWs for truncation geometries I (solid line) and II (dashed line) calculated from FDTD results. Ripples are due to spurious reflections from the absorbing boundaries (second order Higdon).

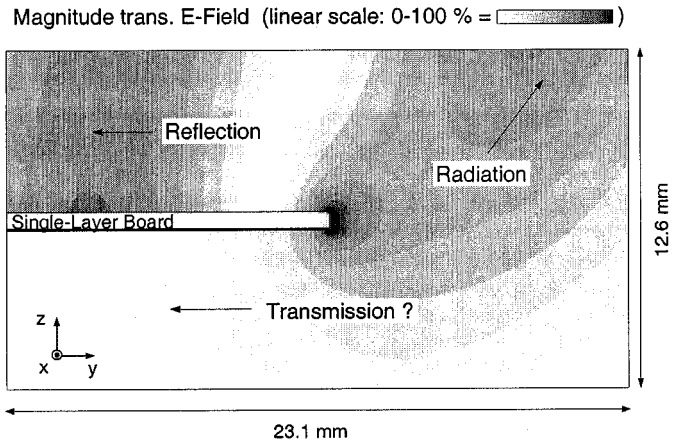

Fig. 17. Snapshot of the transversal electric field strength at the time of TM_0 SW backscattering from the PCB edge. It can be seen that the field stretches out around the edge of the plane which may be an indication that a weak SW-mode may be generated on the backside of the PCB (see text).

In summary, concerning EMC and signal integrity on PCB surfaces one finds the following. 1) TM_0 SW-modes may be present at all frequencies and are easily excited by microstrip discontinuities. 2) The next higher SW-mode (TE_1) is usually of minor concern due to high cutoff. 3) TM_0 SW-modes change their behavior from "quasi-plane-wave" to "trapped" with increasing frequency. 4) Crosstalk due to TM_0 sw-modes becomes important when the mode starts to be "trapped". 5) TM_0 SW-modes are far less reflected by PCB edges than pp-modes and are, therefore, more a concern for free-space radiation than for resonance effects.

Compared to pp-modes, SW-modes seem to bear less dramatic problems for EMC and signal integrity. As long as the TM_0 SW-mode is "quasi-plane-wave" there is, e.g., only reduced potential for crosstalk. However, with rising operating frequencies the plane wave character is more and more lost. A solution to this problem may be the use of low-permittivity materials or thinner substrates if design constraints allow this. Another suggestion is the introduction of electronic bandgap structures for the substrate as presented in [31]. In reality, for both pp- and SW-modes losses in substrates and conductors are present.

Hence it must be kept in mind that the FDTD results presented here slightly overestimate the parasitic effects.

V. Conclusion

In this paper it has been shown that the FDTD method can be applied successfully to the electromagnetic analysis of parasitic slotline, parallel plane, and SW-modes commonly found on printed circuit boards. The parasitic mode conversion process could be visualized using electromagnetic near- and far-field plots. The spatial information of electric near-field maps is especially useful for the prediction of main direction and relative strength of parallel plane and SW-mode excitation. Reflection coefficients of PCB edges have been calculated for both parallel plane and SW-modes. Power loss, crosstalk, and SW-mode characteristics were derived in the frequency domain. A noise field map of a complete PCB showed "hot spots" and "quiet zones" which facilitates placement of sensitive components and bypass capacitors. Throughout the text consequences for EMC and signal integrity of the PCB were discussed and design guidelines for improved performance were derived.

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