Power Deregulation: Eliminatring Off-Chip Voltage Regulation Circuitry from Embedded Systems

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Outline

1. Introduction

2. Technique

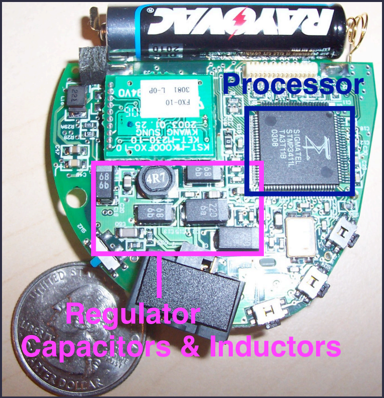
3. Experiments

Power Deregulation

Quick look at the procedure

- Begin with a single core of the chip multi-processor.
- Processor performance diminishes as battery supplied voltage level drops
- Compensate by turning on remaining cores if the system does not meet the required performance level

Motivation



Costs of regulation

- Up to 30% of overall PCB area
- Costs, weight, form factor
- Energy conversion inefficiency
- Instability

Benefits of power deregulation

For manufacturing

- Smaller compact form
- Integrate more features and design flexibility
- Cost saving

Reliability gains

- Possibility of circuit breakdown from long time scale degradation
- Unstable processor voltage due to I-R switching activity

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Power deregulation built upon the following technologies

Dynamic Frequency Scaling

- Operating frequency adapt to changing battery voltage
- Frequency determined by function of V_{DD}
- Power gating

Chip-level multiprocessors

- Already commonly used in general-purpose and embedded computing applications
- Many multimedia applications exhibit high level of parallelism
- Greater parallelism means more performance gained from power deregulation technique
- Power deregulation is designed for embedded systems equipped with multi-core processors

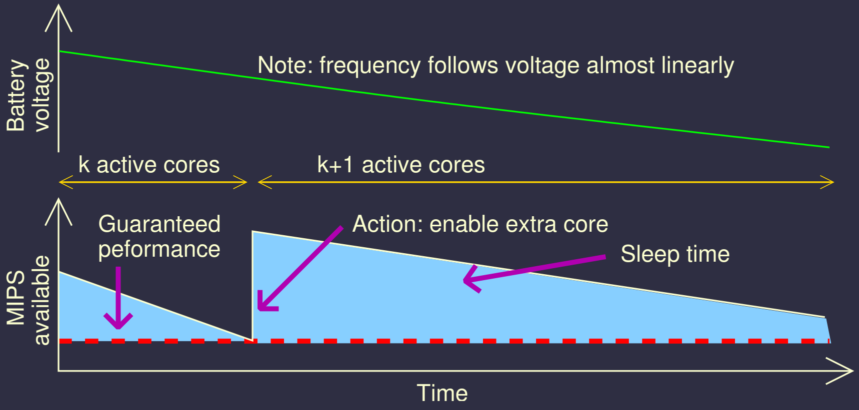
Related Works

Many including Telos sensor node have shown that embedded systems can operate directly from raw battery outputs without voltage regulation

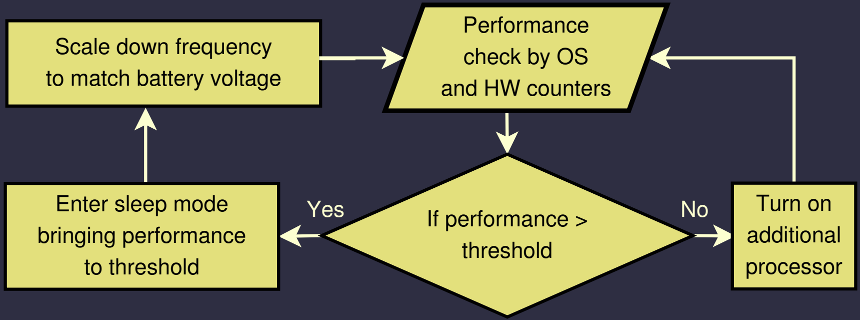
Means of minimizing power dissipation

- Telos approach applies low operating voltage to a single-core processor (underclocking), which means low performance
- Power deregulation maintaining minimal performance level and preventing leakage power (both static and dynamic) by utilizing sleep mode

Power deregulation over time



Power deregulation procedure



Performance threshold & power saving

Performance requirement

- 85% performance boundary set for calculation purpose
- Performance level maintained at its minimum

Sleep mode

- At performance level greater than 85%, task can be done early
- Sleep mode used to conserve power for remaining time
- Even static power can be conserved

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Experimental setup

Simulation environment

- M5 multiprocessor simulator
- DEC Alpha 21164 (EV5) model simulation
- Basic instruction set architecture similar to RISC architectures
- Reconfigured to pipelined in-order processor to better represent embedded systems

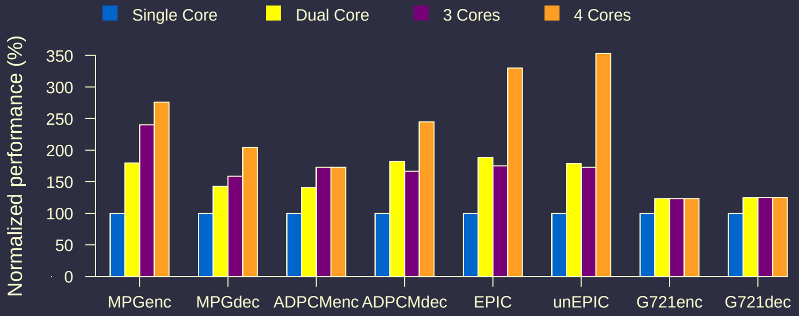
Power modeling

- Baseline architecture: nominal V_{DD} of 3.3 V at 500 MHz
- Computation of both dynamic and static power
- Sleep mode consideration applied

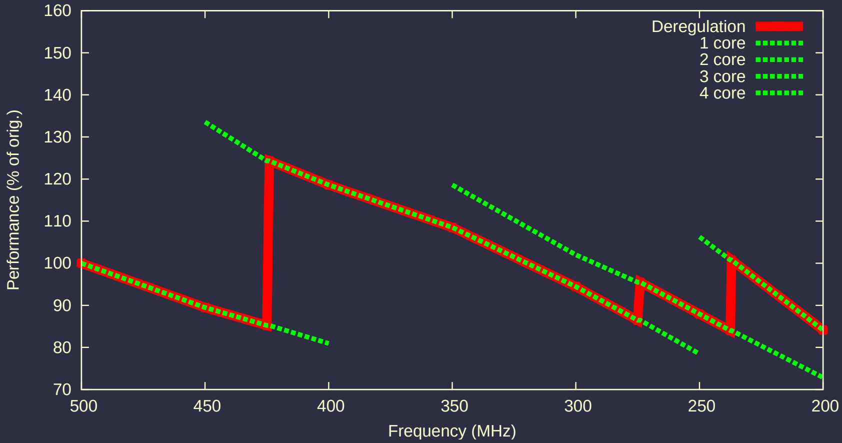
Performance benchmarks

Multithreaded applications

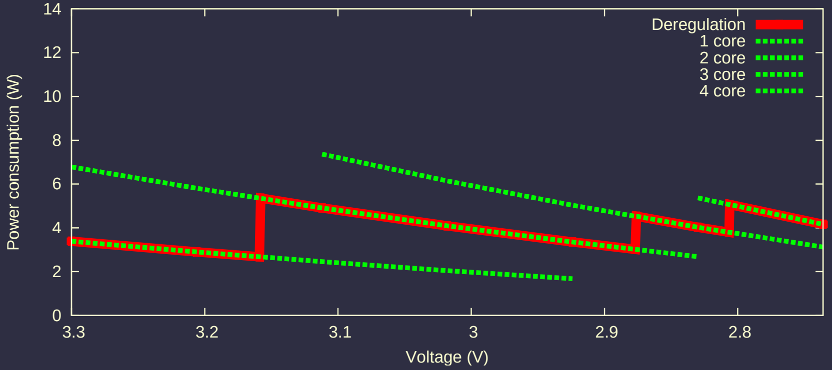
- ALPBench - MSSG MPEG-2 encoder and decoder
- MediaBench - ADPCM, EPIC image, and G721 voice compression



Relative performance for MPEG-2 decoder

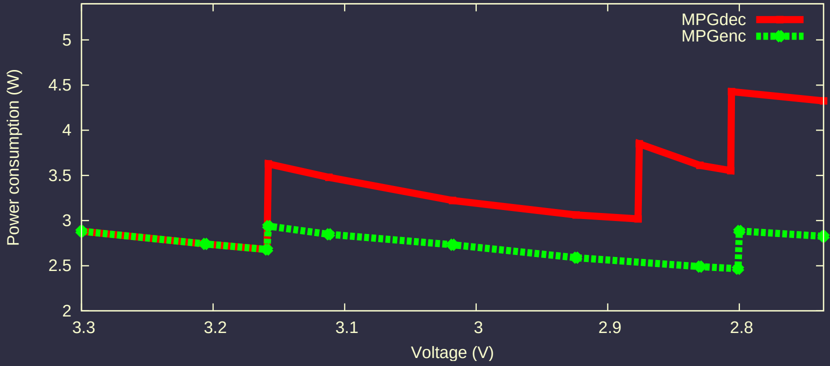


Power dissipation for MPEG-2 decoder



- Variation of power consumption during lifetime of the battery

Power dissipation with sleep mode power saving



Findings

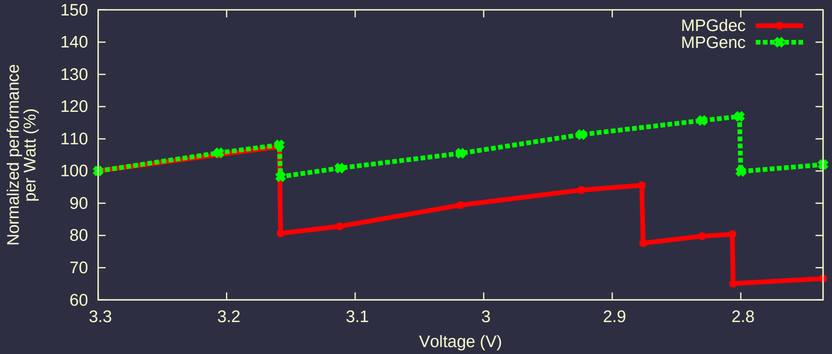
Deregulated system has similar transition patterns for both performance and power metrics

Transition points depend on parallelism efficiency for different benchmarks

Higher parallelism application comprises, transition points are observed at lower voltage points

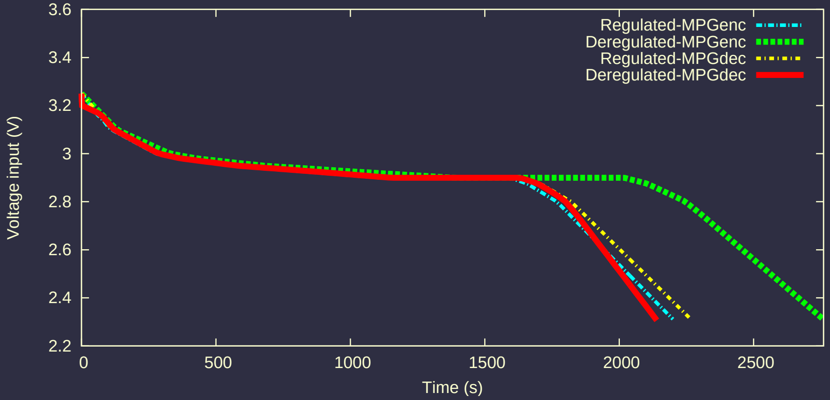
Thus, showing higher performance per Watt

Relative performance per Watt

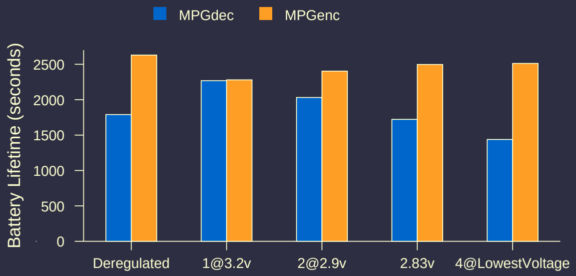


For MPGenc, Performance per Watt increases as voltage decreases and number of processor increases

Battery discharge curve on Li/MnO_2 battery



Battery lifespan comparison with regulated setups



Higher parallelism efficiency leads to greater potential battery lifetime as number of processors increase

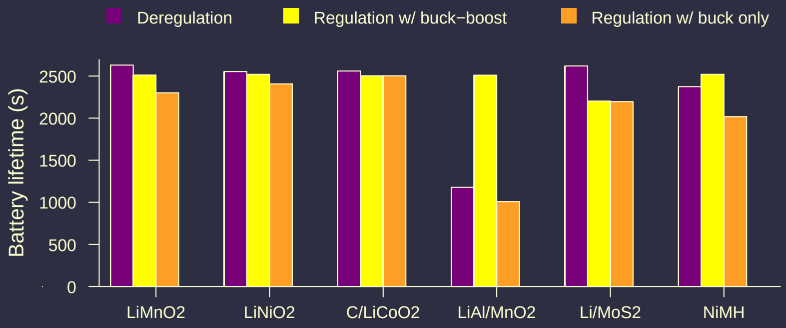
Battery lifespan - buck-boost effect

Buck-Boost and Buck-only Effect

- Conversion efficiency of 85% assumed for regulation
- Buck converter for voltage regulation
- Buck-Boost allows battery utilization at a voltage beyond minimum level demanded by CPU
- Full use of battery energy is assumed for buck-boost model
- Deregulated system performs best in almost all cases

Simulation results for other battery technologies

Battery Technology	Li/MnO_2	$LiNiO_2$	$C/LiCoO_2$	$LiAl/MnO_2$	Li/MoS_2	NiMH
Voltage Supply Range (V)	3.25–2.3	4.25–2.9	4.0–3.15	3.05–1.85	4.5–2.5	2.76–1.84
Critical Region at (V)	2.9	3.95	linear	2.5	linear	2.56



Voltage level at plateau in discharge curve

- Significant factor in determinant comparable battery life
- Optimal if the highest point of performance per Watt is observed at this level

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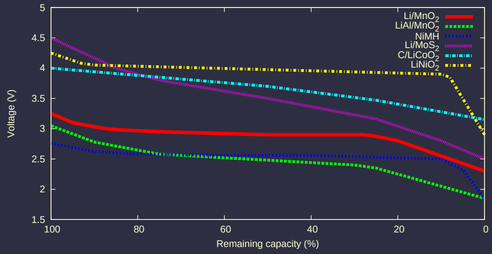

Summary

Power Deregulation

Additional core activation to compensate for diminished performance from reducing battery voltage

- PCB area reduction by 30%
- Elimination of regulatory components
- Comparable battery life span to regulation systems

Sufficiently high parallelism efficiency is required

Acknowledgments

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