Reliability, Thermal, and Power Modeling and Optimization

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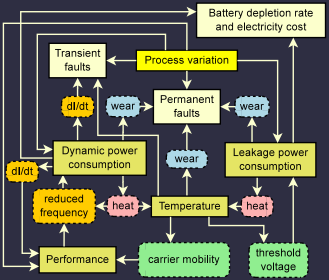

Battery depletion rate and electricity cost
Transient faults
Process variation
dI/dt
wear
Permanent faults
wear
Dynamic power consumption
wear
Leakage power consumption
dI/dt
reduced frequency
heat
Temperature
heat
Performance
carrier mobility
threshold voltage

Intended audience for tutorial

Researchers and designers who are interested in, but new to, temperature-dependent integrated circuit and embedded system reliability modeling and optimization.

Goals

Suggest sources of new reliability research problems.

Explain relationships among power consumption, temperature, and reliability.

Indicate the difficulty of generalized reliability modeling and optimization.

Request reliability modeling anecdotes for public repository.

My background and perspective

Integrated circuit power, thermal, and reliability modeling and optimization.

Embedded system reliability modeling during design and synthesis.

Tutorial sections

1. Indicate state and trends in research field
2. Power, temperature, and reliability
3. Trade-off between sophistication and complexity in reliability modeling and optimization
4. Reasons for difficulty of developing general models

Tutorial subsections

1. Indicate state and trends in research field
    - State of reliability research field
    - Sources of new research problems
    - Reliability problem taxonomy
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Historical development of research fields

Case studies.

Modeling and optimization.

Generalized and automated modeling and optimization.

State of reliability research

Embedded systems reliability

- Case studies.
- Variation in environmental conditions and applications makes generalization difficult.
- Caveat: Some areas within embedded system design are better understood than others.

Integrated circuit reliability

- Empirical models of device-level fault processes.
- Well-developed theory for system-level reliability estimation, as long as component fault rates are known.
- Ongoing work on (automated) system-level reliability modeling, monitoring, and optimization.
  - Complicated by impact of on-line adaptation on fault/wear rates.

Recent academic IC and system reliability research

Reliable nanoscale logic (DeHon, Jha, Orailoglu, et al.) and system (Atienza, Benini, De Micheli, et al.) design.

Reliability-aware IC operating parameter and power consumption state optimization: Eles, Pop, et al.

Soft error protection and modeling: Dutt, Narayanan, Xie, et al.

Architectural techniques for improved reliability: Adve, Alameldeen, Austin, Bertacco, Falsafi, Mahlke, Mudge, Skadron, et al.

Trading off correctness for improvements in other quality metrics: Palem, Memik, et al.

Circuit failure prediction and self-tuning: Cao, Mitra, Wei, et al.

Reliability-aware (networked) embedded system design and synthesis: Coskun, Shang, Teich, Thomas, Dick, et al.

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Sources of new research problems

Changes in applications.

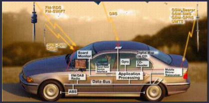
Changes in implementation technologies.

Application trends influencing reliability

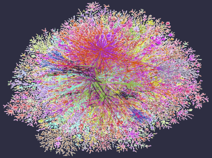
Inexpensive computers in harsh environments.

Figure from http://wsn-security.info.

Battery-motivated energy constraints.



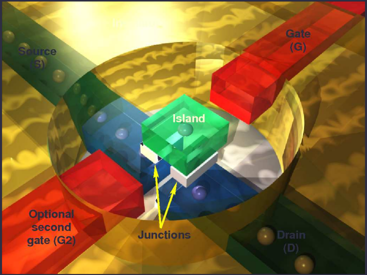
Use in safety-critical applications, e.g., transportation and medical devices.

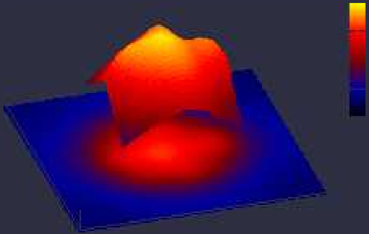


Networked systems.

Figure from Huafeng Xie.

Technology trends influencing integrated circuit reliability





Use of nanoscale devices.

More variation.

Better sensors.

Power density, variation increase.

More cores.

More devices.

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Specification and design

Responsible for vast majority of in-system faults [Rahman'06].

An error per ∼100 lines of code is considered a very good rate.

What is being done?

- Language design.
- Formal verification.
- Software engineering.
- Operating system and middleware design.
- Hardware synthesis.

See written tutorial summary for citations.

Permanent faults

Many permanent faults related to lifetime wear processes.

Temperature dependent.

Wear state can be estimated or tracked.

However, on-line monitoring/testing impact cost.

Intermittent and transient faults I

Influenced by both controlled and uncontrolled (environmental) conditions.

Examples

- Temperature-dependent timing violations.
- R drop.
- dI/dt.
- C or L crosstalk.

Intermittent and transient faults II

Single-event upsets

- Cosmic rays interact with atoms in atmosphere, producing shower of high-energy neutrons.
- In general, danger increases with process scaling – decreased node capacitance.
- Single particle can trigger multiple upsets.

Influence of parameter variation

Fabrication time

- Cuts into safety margins.
- Changes sensitivity to dynamically varying environmental parameters.
- E.g., reduced threshold voltage increases power density and temperature.

On-line

- Operating parameters influence, and influenced by, wear processes.
- E.g., V_t, are influenced by wear processes.

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2. Power, temperature, and reliability
    - Wear mechanisms
    - Relationships among power, temperature, and reliability
    - Thermal analysis
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Wear mechanisms I

Electromigration.

Dislocation of metal atoms caused by momentum imparted by electrical current in wires and vias.

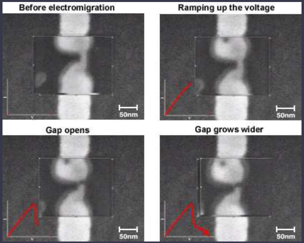

Figure from Taychatanapat, Bolotin, and Kuemmeth.

Wear mechanisms II

Time-dependent dielectric breakdown.

Deterioration of the gate oxide layer: formation of conductive path.

Stress migration

Directionally biased motion of atoms in wires due to mechanical stress.

Negative bias temperature instability

- Electric field dependent disassociation of Si–H bonds at Si–SiO_2 interface.
- Increases threshold voltage.
- Significant for PMOSFETs under negative bias.
- Partially recovers when negative bias is removed.

Wear mechanisms III

Thermal cycling

- Mechanical stress resulting from mismatched coefficients of thermal expansion for adjacent material layers.
- Special class of memory: depends on recent temperature history, not just wear state and environment.

Lifetime estimation of the failure mechanisms

Most mechanisms

Arrhenius equation:

$$MTTF = j_1 e^{\frac{j_2}{T}}$$

- j_1 and j_2: wear process dependent constants.
- T: temperature.

Thermal cycling

Generalized Coffin-Manson eq.:

$$N = \frac{k_1}{(\delta T - T_{th})^{k_2}} e^{\frac{k_3}{T_{max}}},$$

- k_1, k_2, and k_3: constants.
- N: cycles to failure.
- δT: thermal cycle amplitude.
- T_{th}: temperature change threshold.
- T_{max}: maximum temperature during the cycle.

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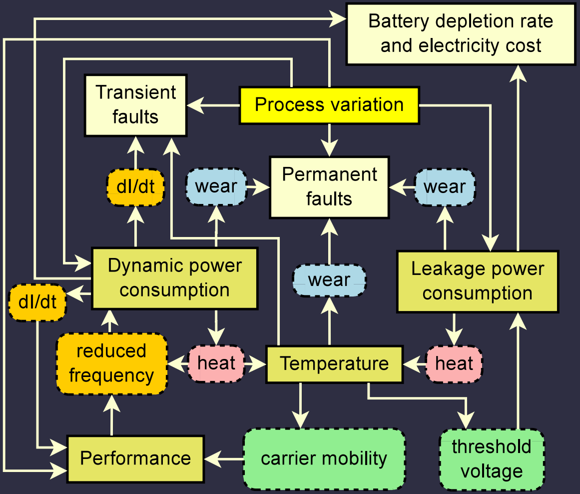
Relationships among power, temperature, and reliability



Required information for reliability estimation

Need

- Thermal profile, which requires
- power profile.

May need temporal distribution or time series, depending on dominant fault processes.

May need current densities.

May need process variation characteristics.

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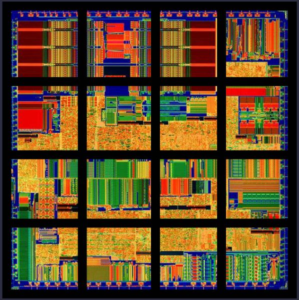
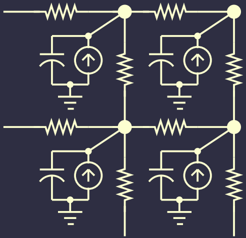
Macroscopic thermal analysis





Partition into 3-D elements (diagram 2-D for simplicity)

Temperature	↔	Voltage
Thermal resistance	↔	Resistance
Heat flow	↔	Current
Heat capacity	↔	Capacitance

Device-level thermal analysis

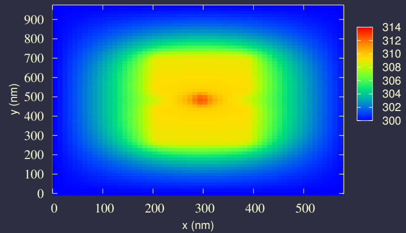
Architectural thermal analysis tools

- Functional-unit level spatial discretization.
- 10–100 µm element sizes.
- 100 µs–1 ms time step sizes.
- Fourier heat flow model.

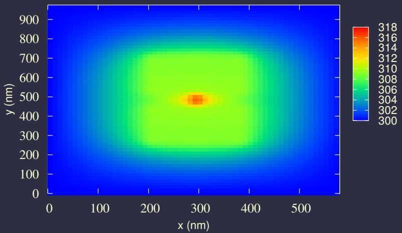
When device length scales shorter than phonon mean free path (∼100 nm), conventional diffusion-based thermal analysis breaks down.

I.e., when "heat particles" interact with the material lattice after traveling short distances.

Need non-Fourier models and analysis for nanoscale devices



Thermal profile of 65 nm FinFET (Fourier heat flow).



Thermal profile of 65 nm FinFET (Boltzmann Transport Equation).

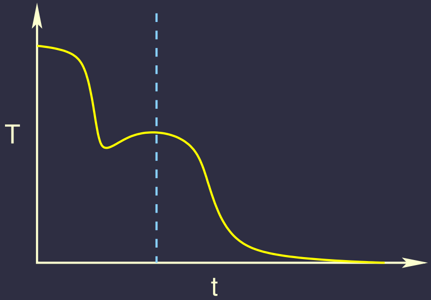
Figures from Zyad Hassan.

Wear-dependent fault processes without other state I

Parameter distribution suffices.

E.g., temperature distribution.

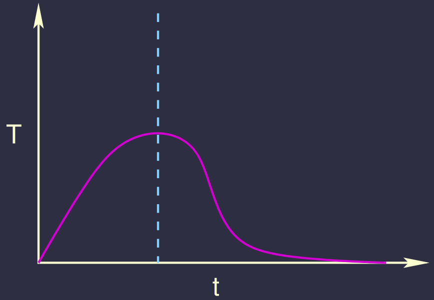
Wear-dependent fault processes with other state



E.g., thermal cycling.

Aggregate parameter distributions insufficient.

Wear-dependent fault processes with other state



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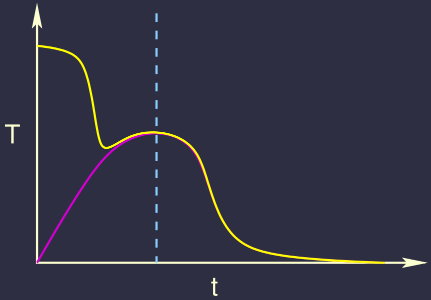
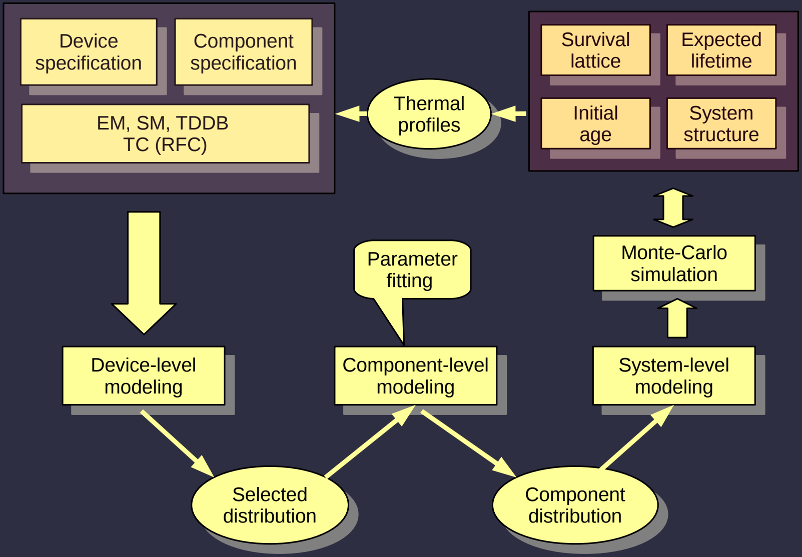
Wear-dependent fault processes with other state



E.g., thermal cycling.

Aggregate parameter distributions insufficient.

Sketch of power, thermal, and reliability modeling flow



Device specification

Component specification

EM, SM, TDDB
TC (RFC)

Thermal profiles

Survival lattice

Expected lifetime

Initial age

System structure

Monte-Carlo simulation

Parameter fitting

Device-level modeling

Component-level modeling

System-level modeling

Selected distribution

Component distribution

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    - Hierarchy of modeling and optimization techniques
    - Complexity–quality metric trade-off

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Example hierarchy of modeling and optimization techniques

Ignorance.

Static fault rates, no redundancy.

Variable fault rates (wear modeling), redundancy.

Variable-rate environmental parameter dependent wear modeling, redundancy.

Sensor-based estimation of environmental parameters, on-line fault detection and adaptation.

Is more sophisticated better? Not always.

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Complexity–quality metric trade-off: What is optimal?

Common proposal

- Use more sophisticated modeling and adaptation techniques to allow tighter guardbands.
- Supports improved performance, reliability, or cost (pick any two).

Costs of sophistication

- Do designers need to spend time learning and remembering complex new concepts?
- Is the design process made more difficult or changed?
- Is debugging or analysis made more difficult?
- Does the technique impose overhead (performance, power, etc.)?

Simplicity does not preceed complexity,
but follows it.

Alan Perlis

Promising directions

Studies that indicate the operating conditions necessary for a particular type of fault to matter.

Lets designers ignore things that should be ignored.

Generalized or automated modeling techniques.

Opportunities for design automation researchers.

Low-level, low-complexity techniques that reduce a particular reliability problem.

- Multiple unidirectional current vias for electromigration.
- Change in packaging for α particles.

System-level performance enhancement infrastructure that happens to also support adaptation for reliability.

Motivate use before it is too late.

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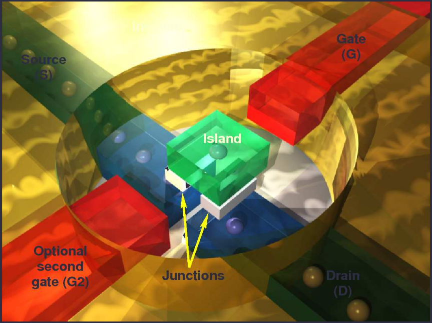
    - Example technology-specific reliability problems
    - A plea for anecdotes

Random background offset charge effects



Defects near gate act trap charge carriers.

Two close defects? Charge carrier tunnels between them.

Result: Randomly changing I–V curve phase.

Wide range of timescales, ns–many hours.

Can general approach solve this?

Maybe, but less efficient than one based on understanding of cause of faults.

Rain


Courtesy of JMEX60 / GNU Licensing

Inexpensive sensors deployed in harsh environments.

Many possible reliability problems.

Difficult to predict and prepare for each.

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A plea for anecdotes

Hypothesis

System designers often encounter reliability problems that are difficult to predict, but obvious in hindsight, and therefore rarely published. As a result, these problems remain difficult to predict.

Offer

I will maintain an (anonymized if requested) list of reliability problem anecdotes to help designers determine the most likely problems. Email dickrp@eecs.umich.edu.

Case studies are a foundation.

Our relevant tools and work

Reliability modeling and optimization in distributed sensing systems: Bai et al., DATE'11.

Nano- to system-scale integrated circuit thermal analysis software: N. Allec, et al., "ISAC2: Incremental self-adaptive chip-package thermal analysis software, version 2," ISAC2 link at http://ziyang.eecs.umich.edu/projects/isac and http://eces.colorado.edu/~hassanz/ThermalScope.

Thermal and reliability modeling survey: Brooks et al., IEEE Micro'07.

Thermal and reliability modeling and optimization techniques and software: Multiple. See http://robertdick.org/publications/.

Thanks!

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Thank you for attending!

More information at http://robertdick.org/.